

VM8G Block Diagram Intel Discrete GFX

VER : F3B

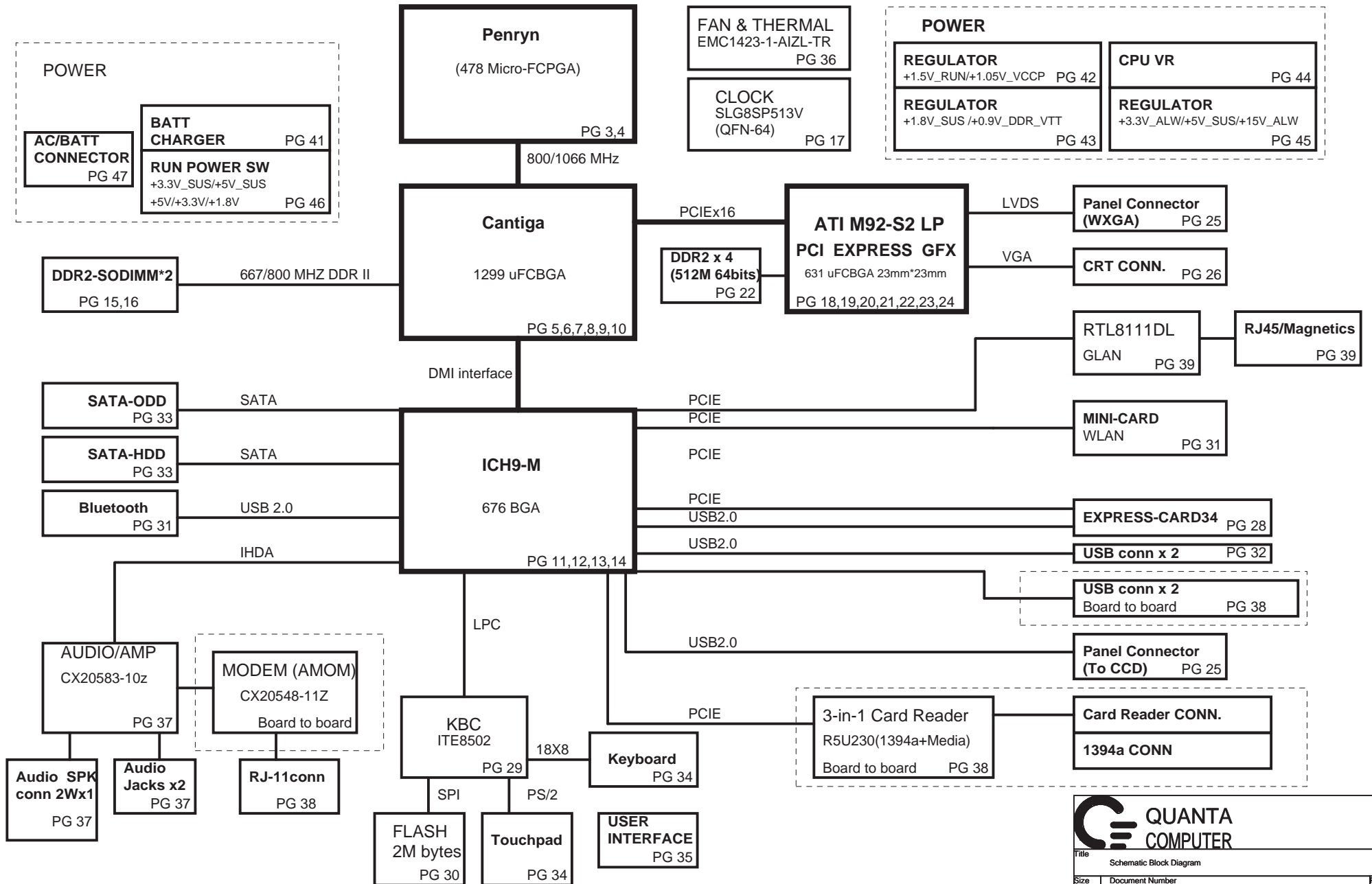




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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,25,30,39,41,42,43,44,45,49,50	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,29,30,35,39,40,41,43,45,46,47	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	42,43,45,46,47,49	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	25,45,46	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	39	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,32,35,44,45,46,49,50	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,19,25,28,35,42,44,46,49	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,42,43,46,49	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,43,46	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,26,33,34,35,36,37,46,50	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,6,8,9,11,12,13,14,15,17,19,25,26,27,28,29,31,33,35,36,37,39,46,50	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,28,31,42,46,50	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,42,50	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,44	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	25	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	33	Module Power	MODC_EN#	
+5V_HDD	+5V	33	HDD Power	HDDC_EN#	
+PBATT	+10V~+17V		MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V		SECOND BATTERY	CHG_SBATT	
+1.1V_GFX_PCIE	+1.1V	20	GFX PCIE POWER	GFX_RUN_ON	
+VCC_GFX_CORE	+0.9~+1.1	20,23,49	GFX CORE POWER	GFX_RUN_ON	

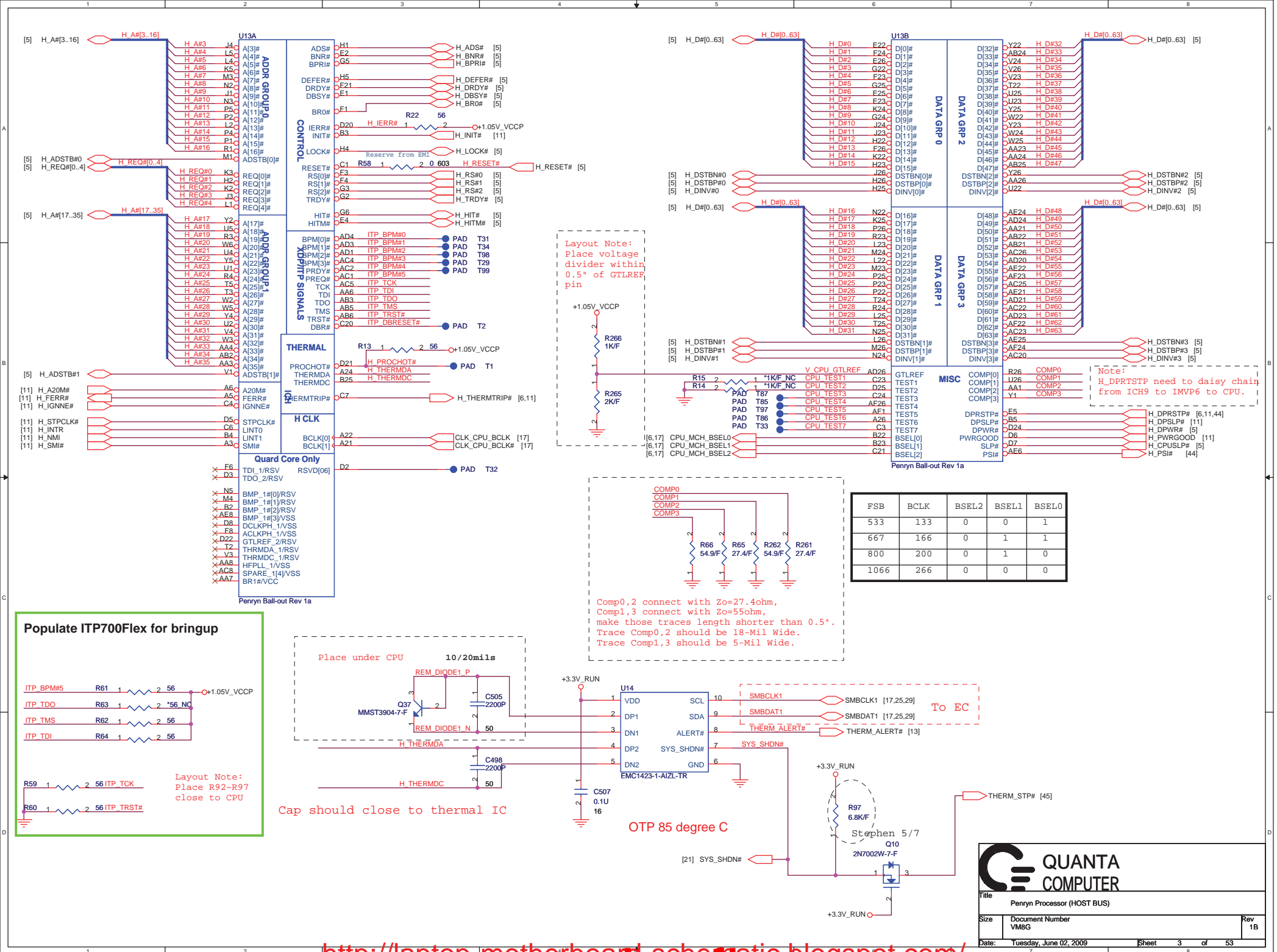
GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

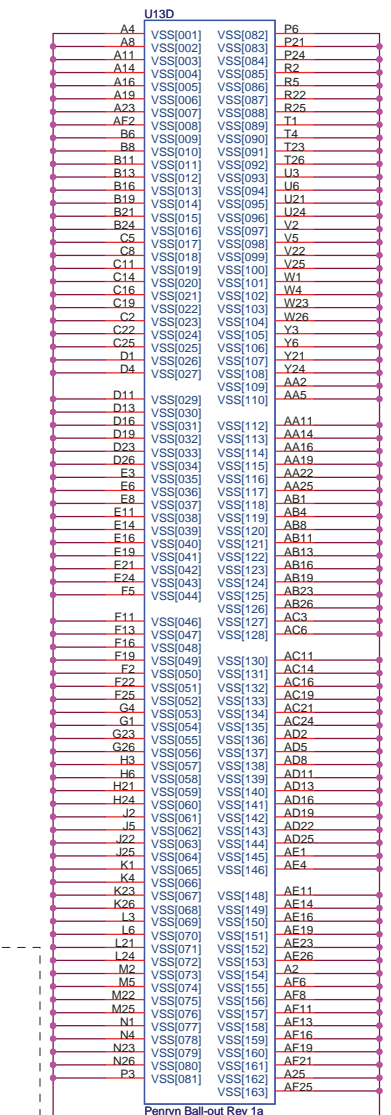
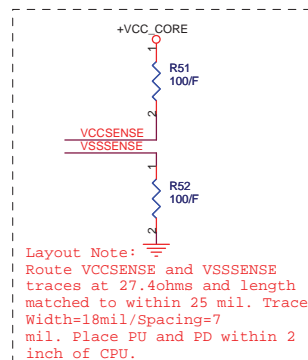
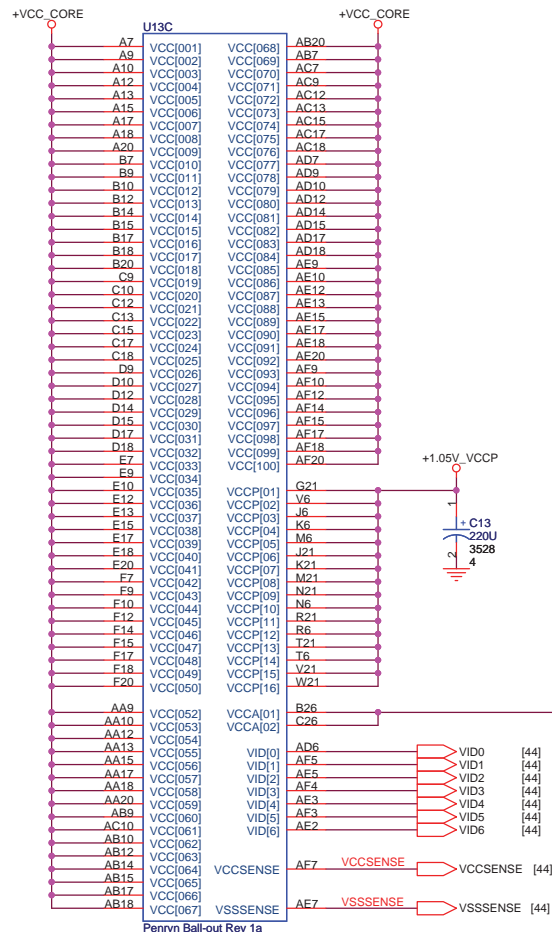
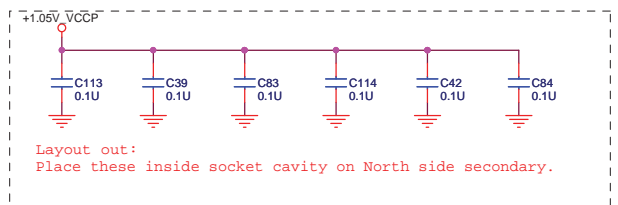
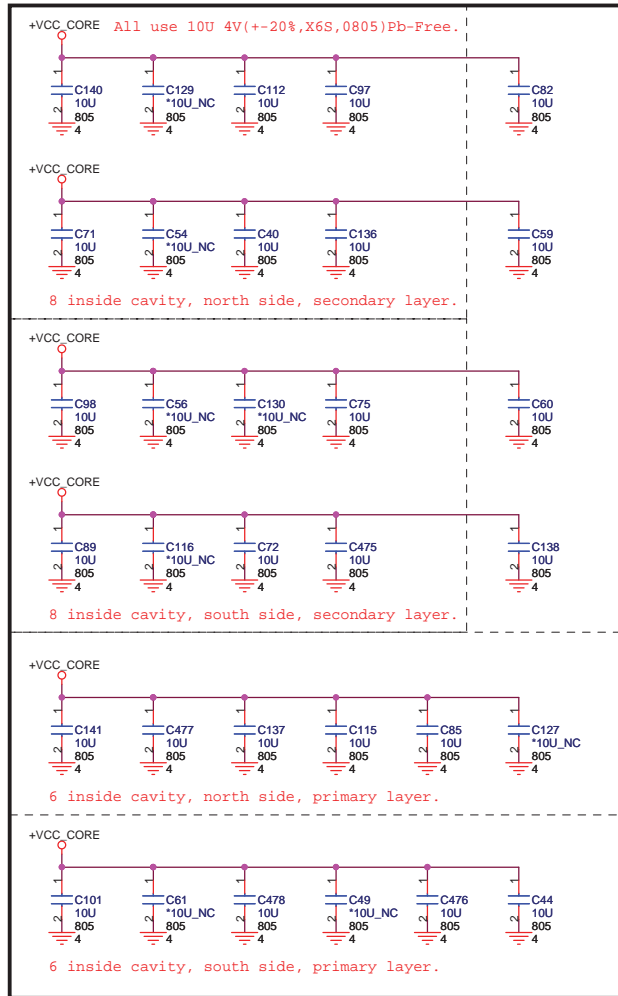

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COMPUTER**

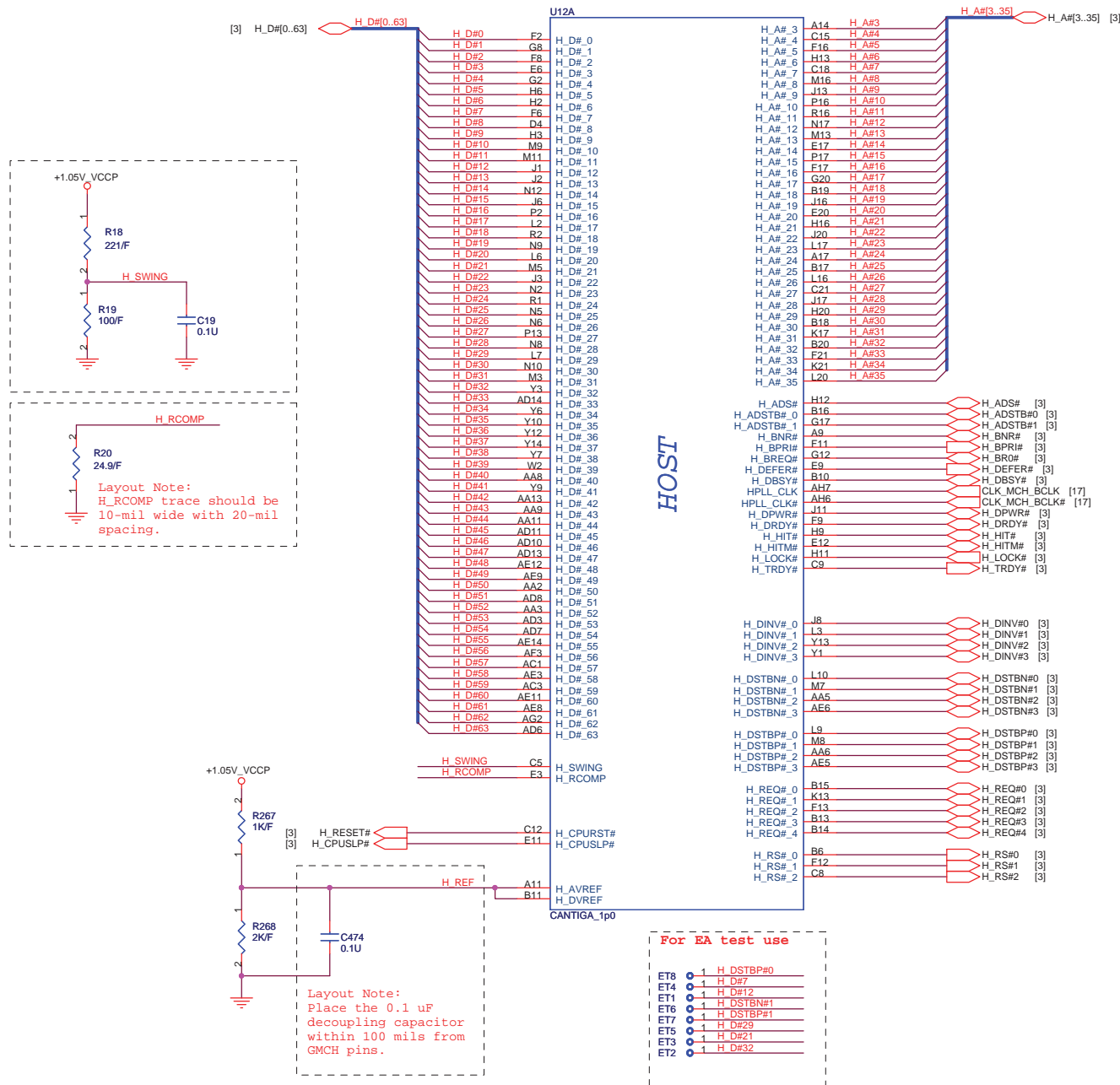
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Size: Document Number VMBG Rev 1B

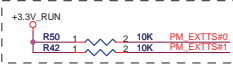
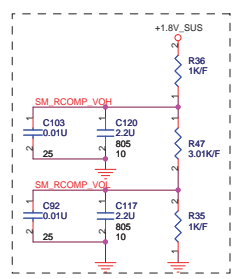
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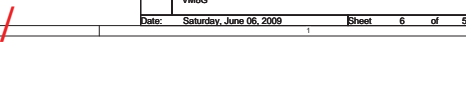
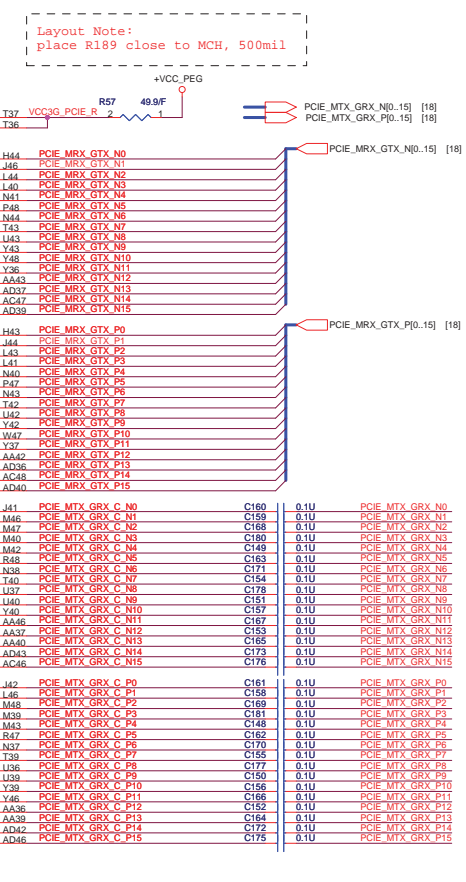
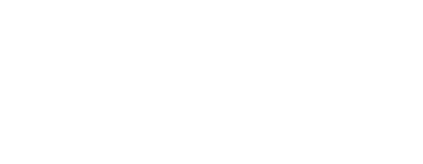
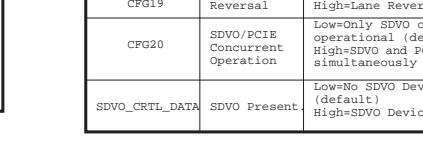
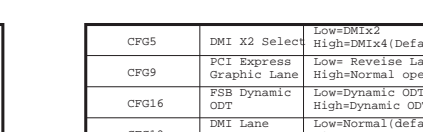
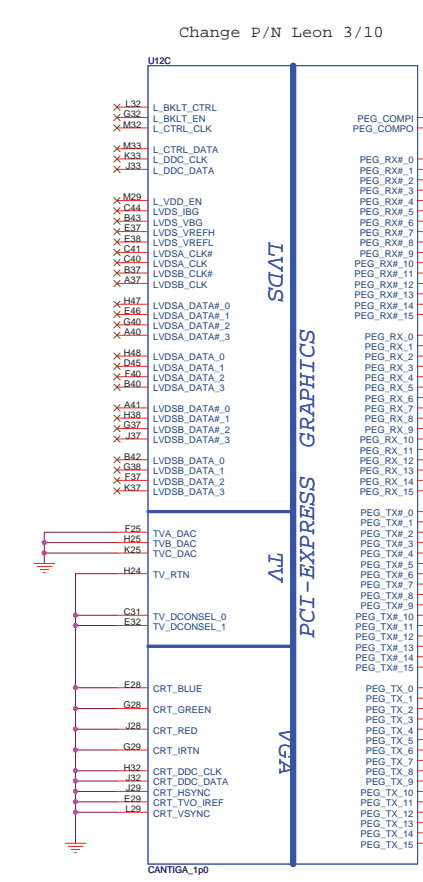
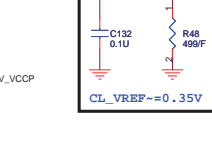
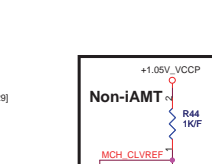
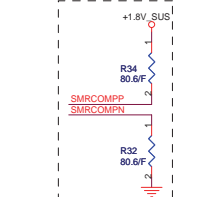
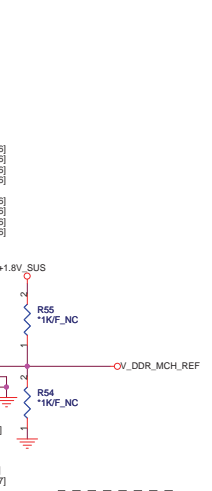
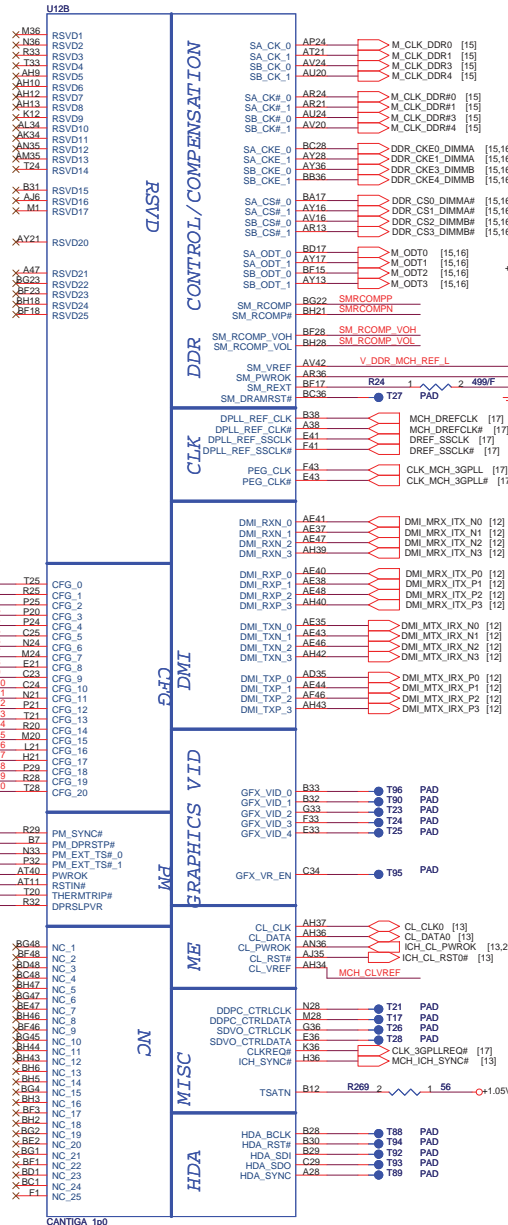
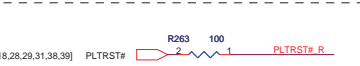
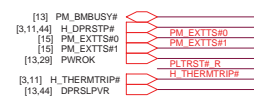
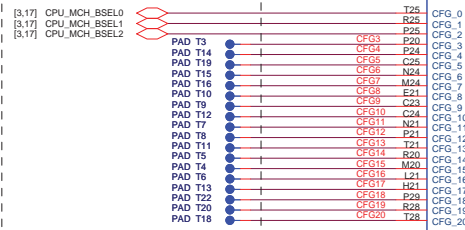


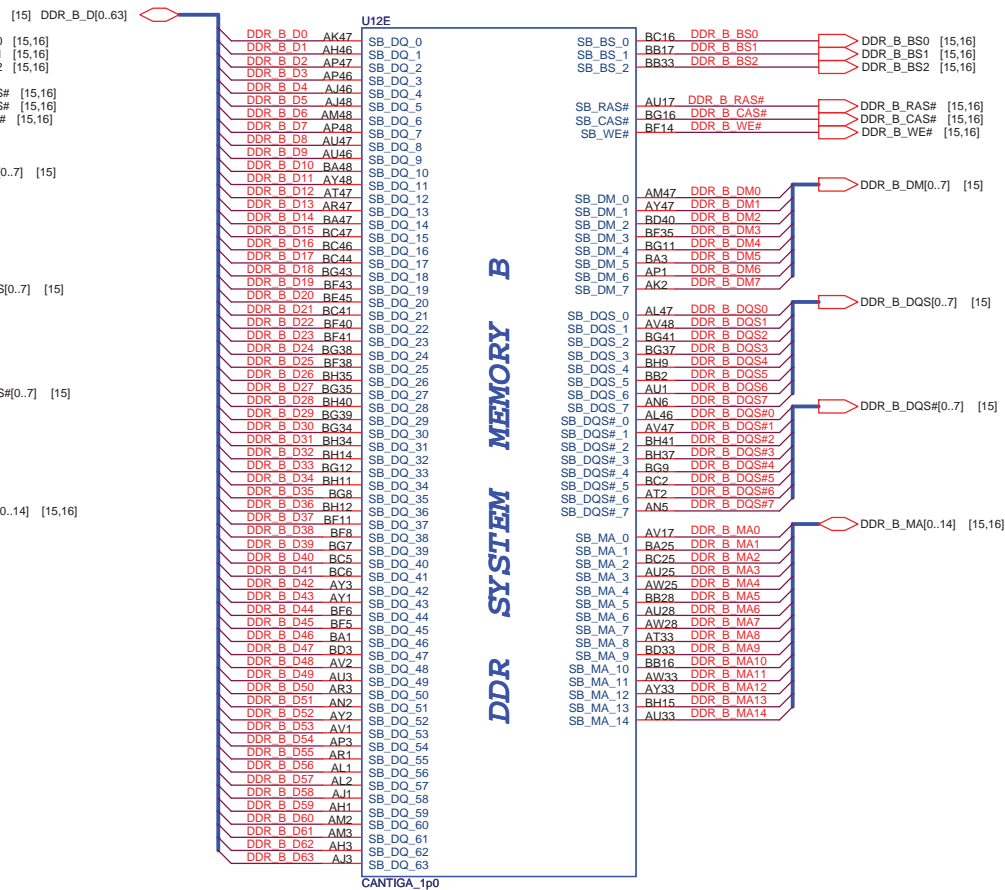
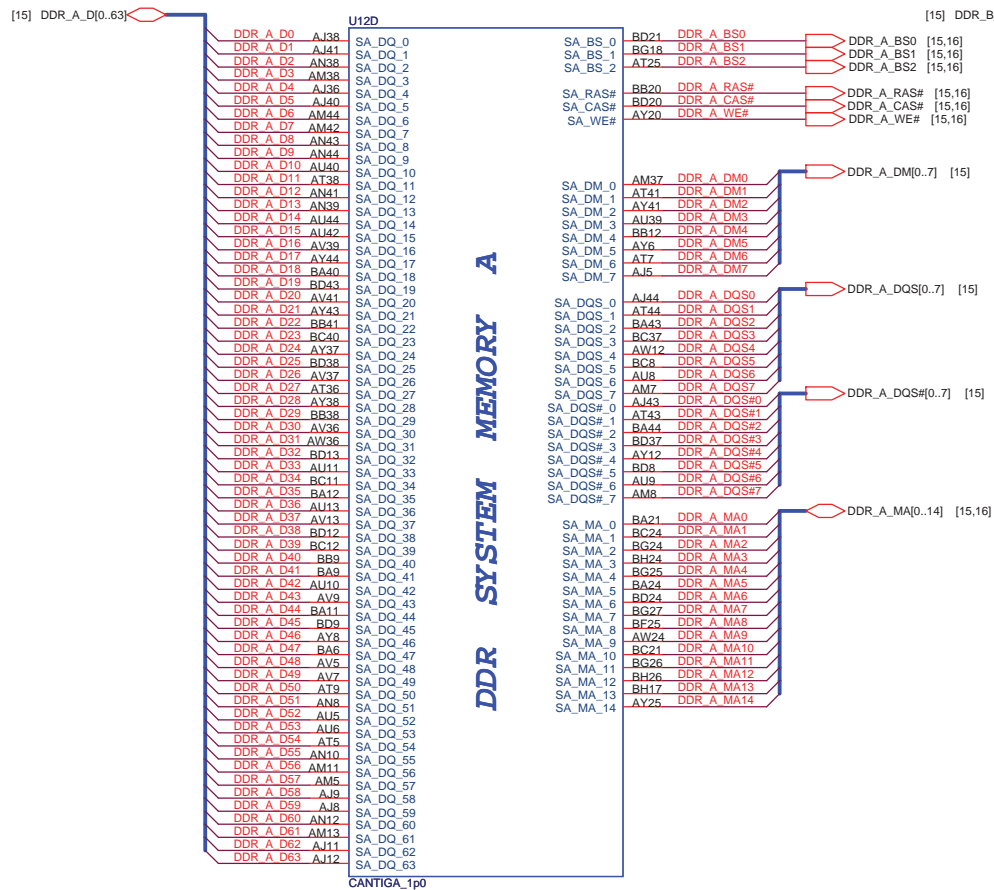


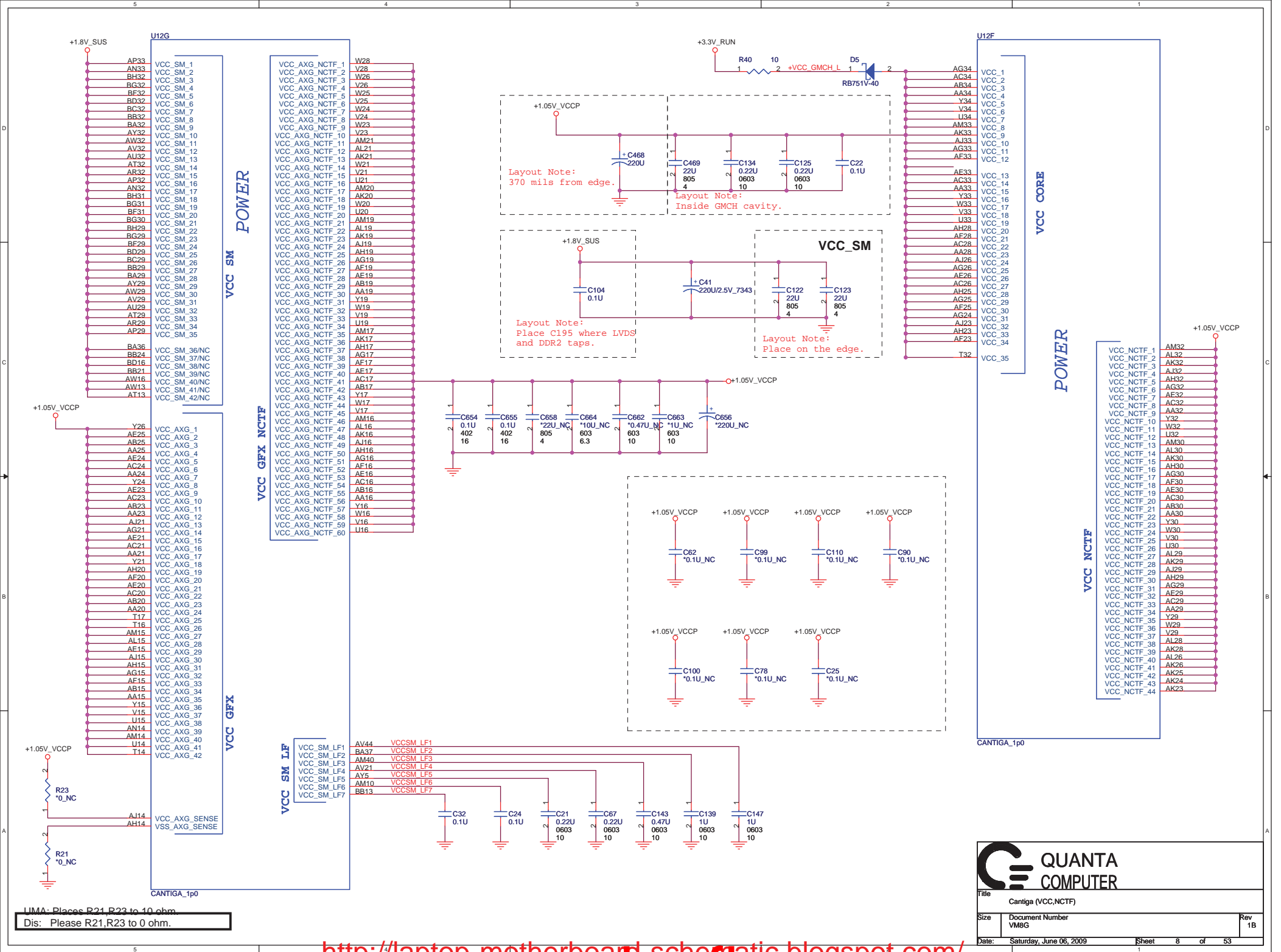
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Size VM8G	Document Number	Rev 1B
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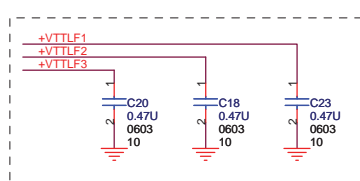
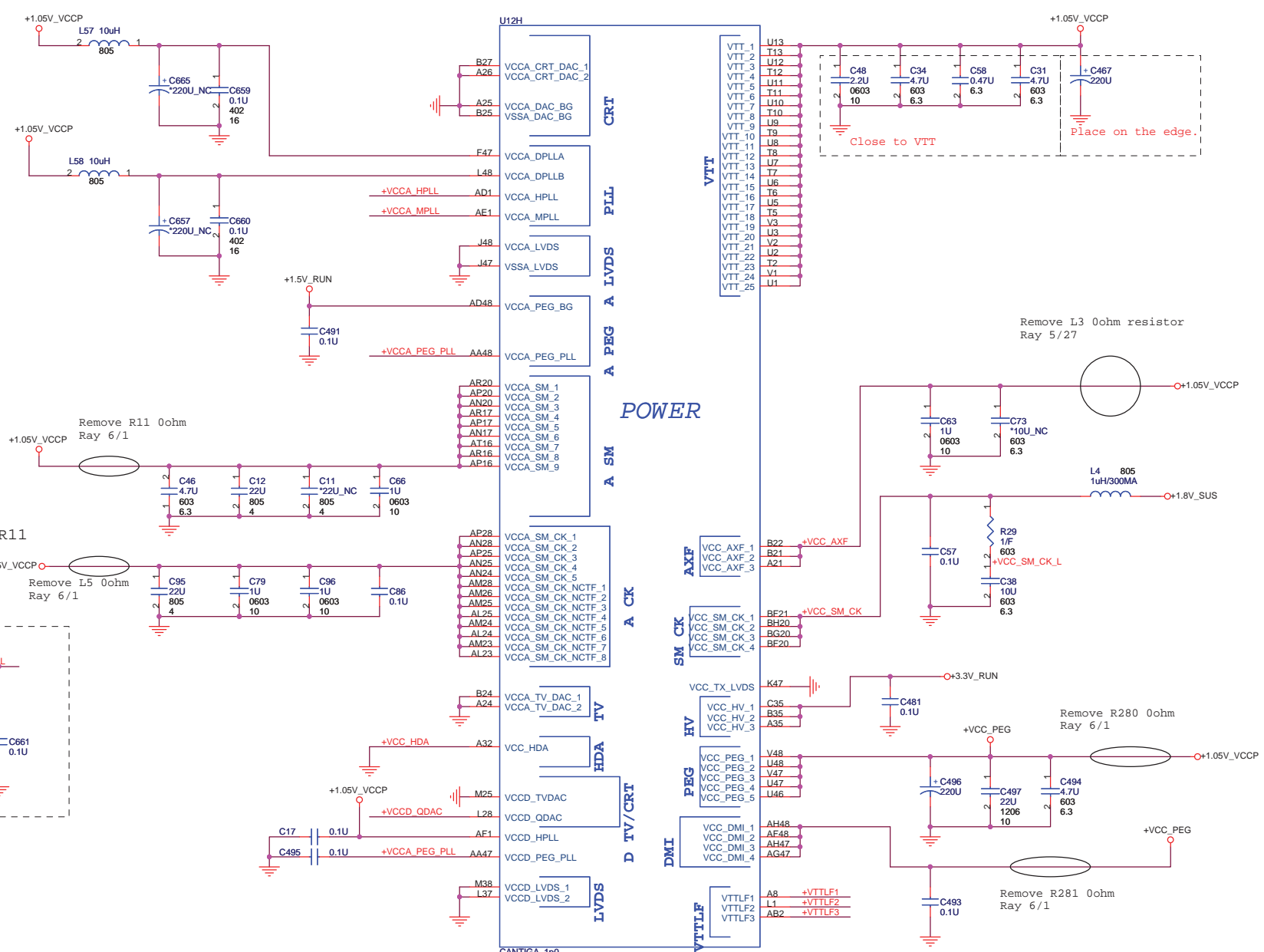
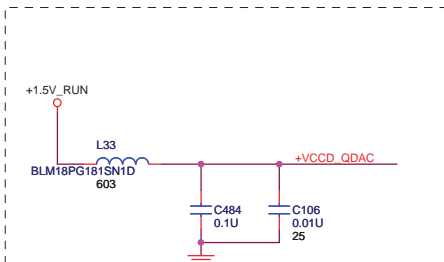


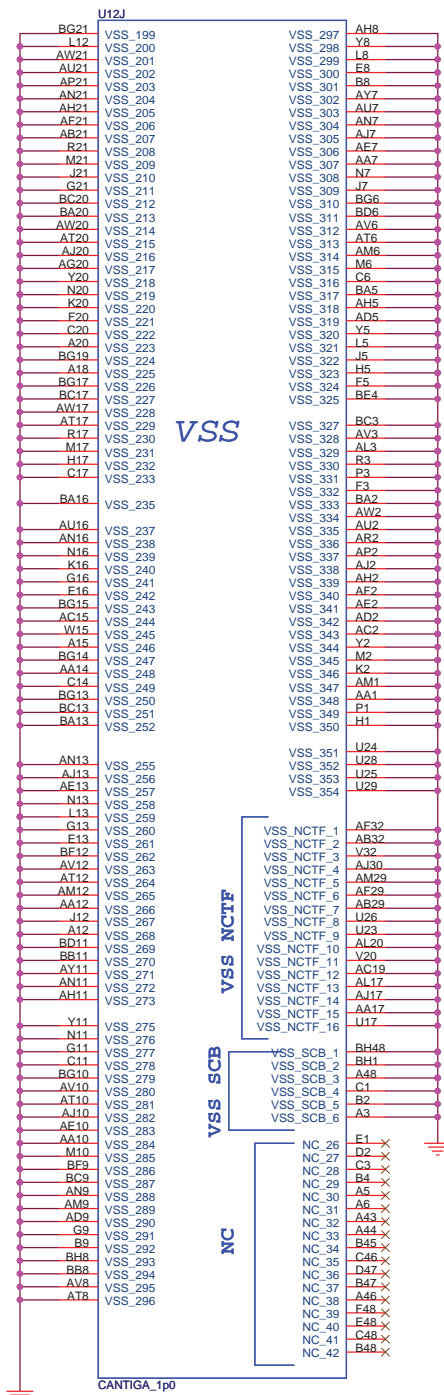
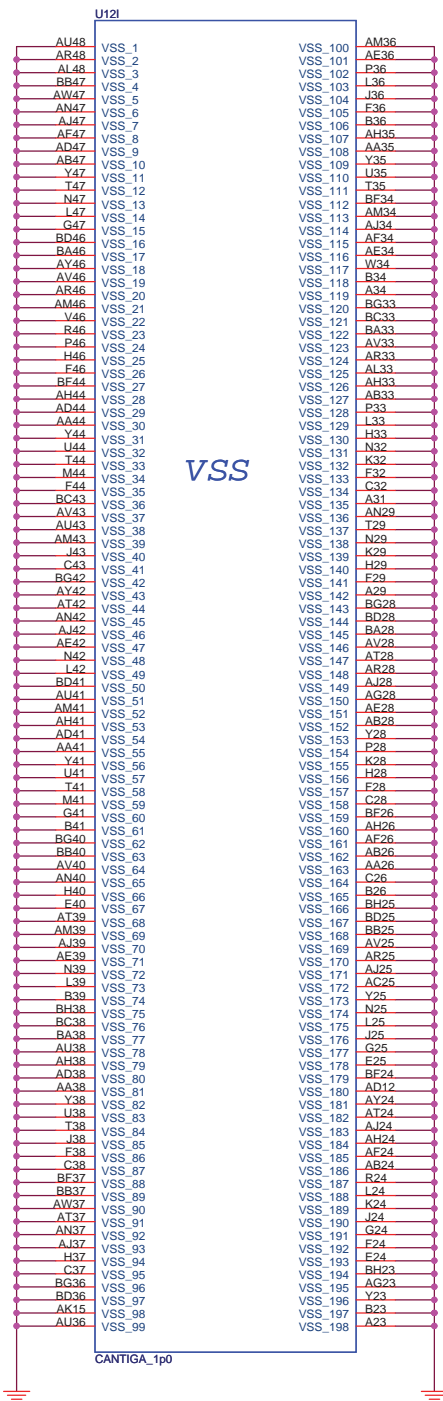
Layout Note:
Location of all MCH_CFG strap resistors need to be close to minimize stub.




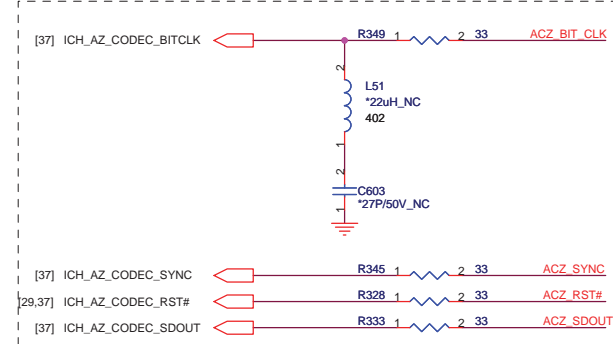
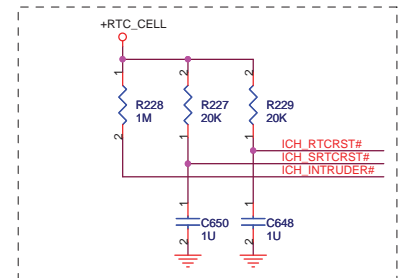
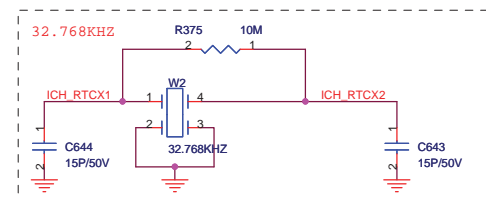




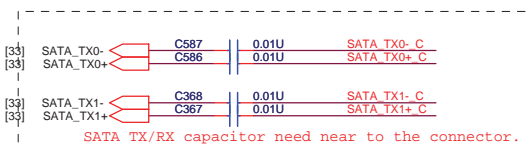




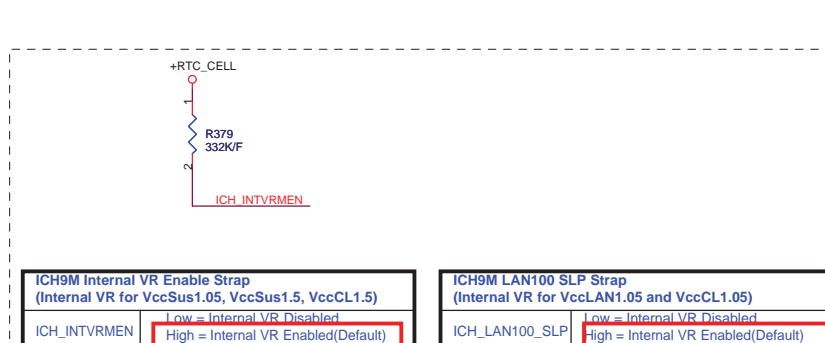
 QUANTA COMPUTER			
File: Cantiga (VSS)			
Size: VM8G	Document Number		Rev: 1B
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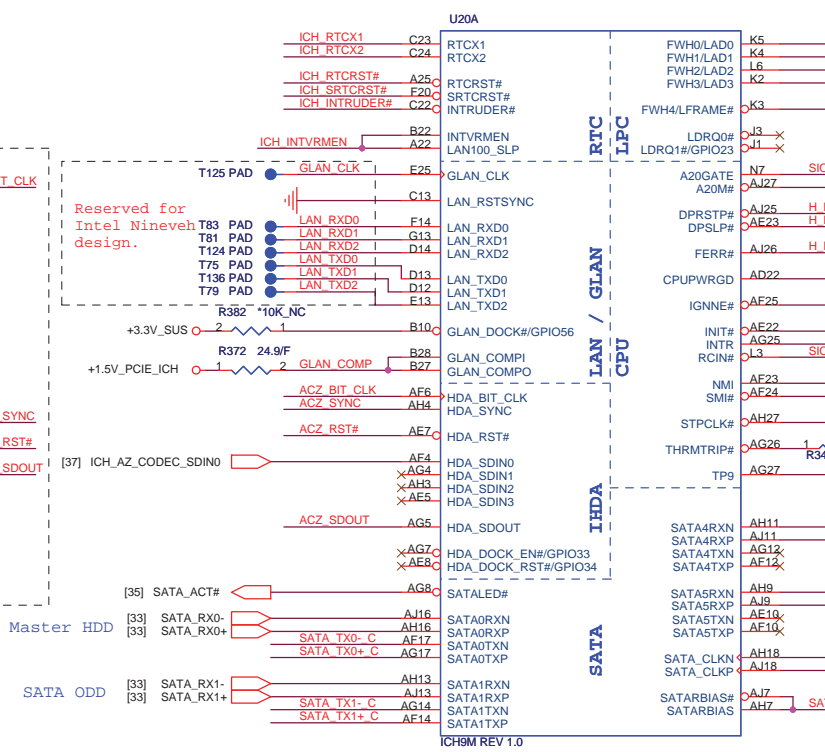
Place all series terms close to ICH9 except for SDIN input lines, which should be close to source.



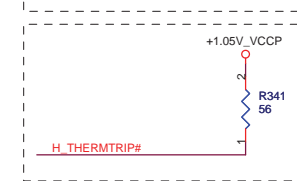
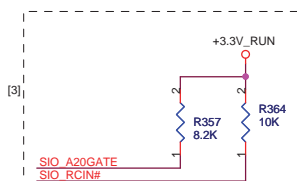
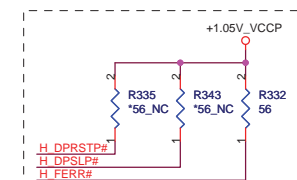
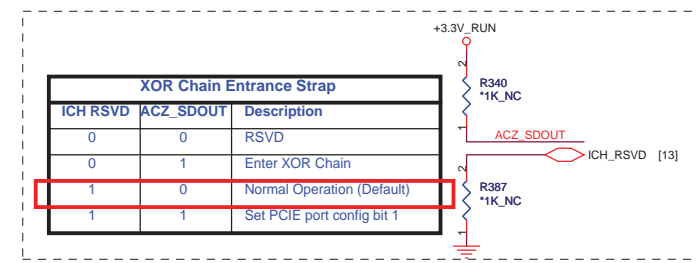
SATA TX/RX capacitor need near to the connector.



Low = Internal VR Disabled
High = Internal VR Enabled(Default)



ICH9M REV 1.0



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File: ICH9-M (CPU,SATA,LPC,LAN,CODEC)

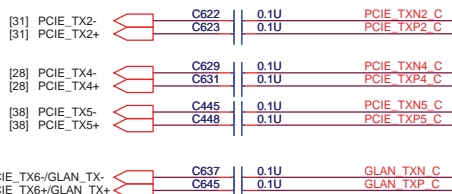
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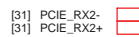
Rev: 1B

Place TX DC blocking caps close ICH9.

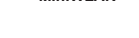


Boot BIOS Strap			
		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

MiniWWAN



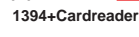
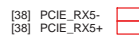
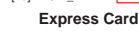
MiniWLAN



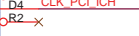
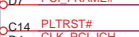
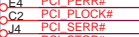
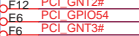
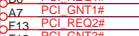
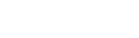
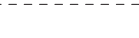
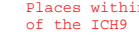
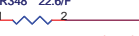
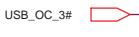
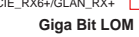
MiniWPAN



Express Card



Giga Bit LOM



U20D



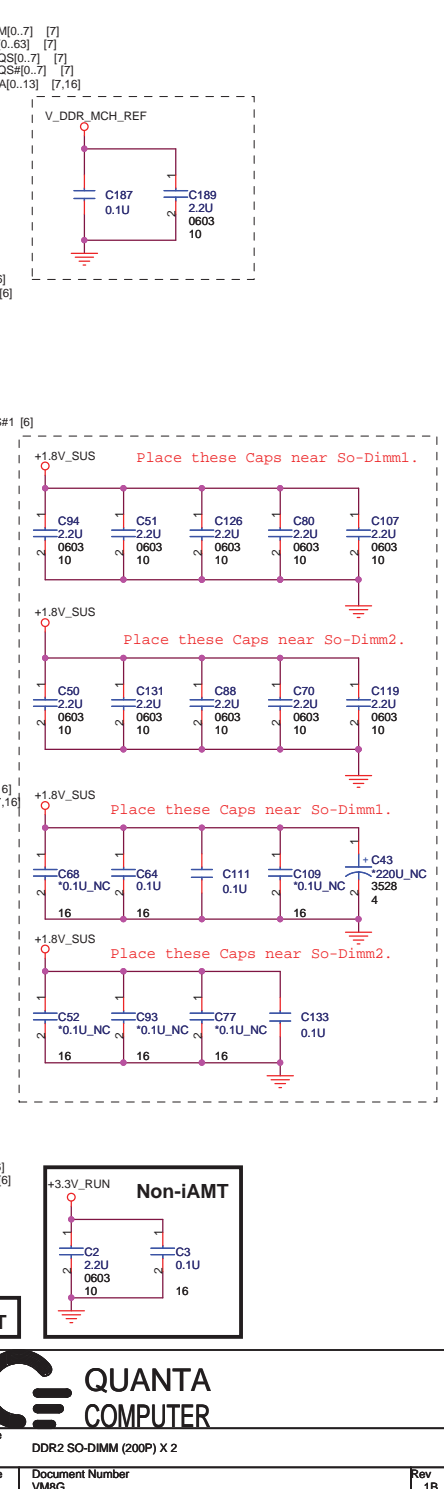
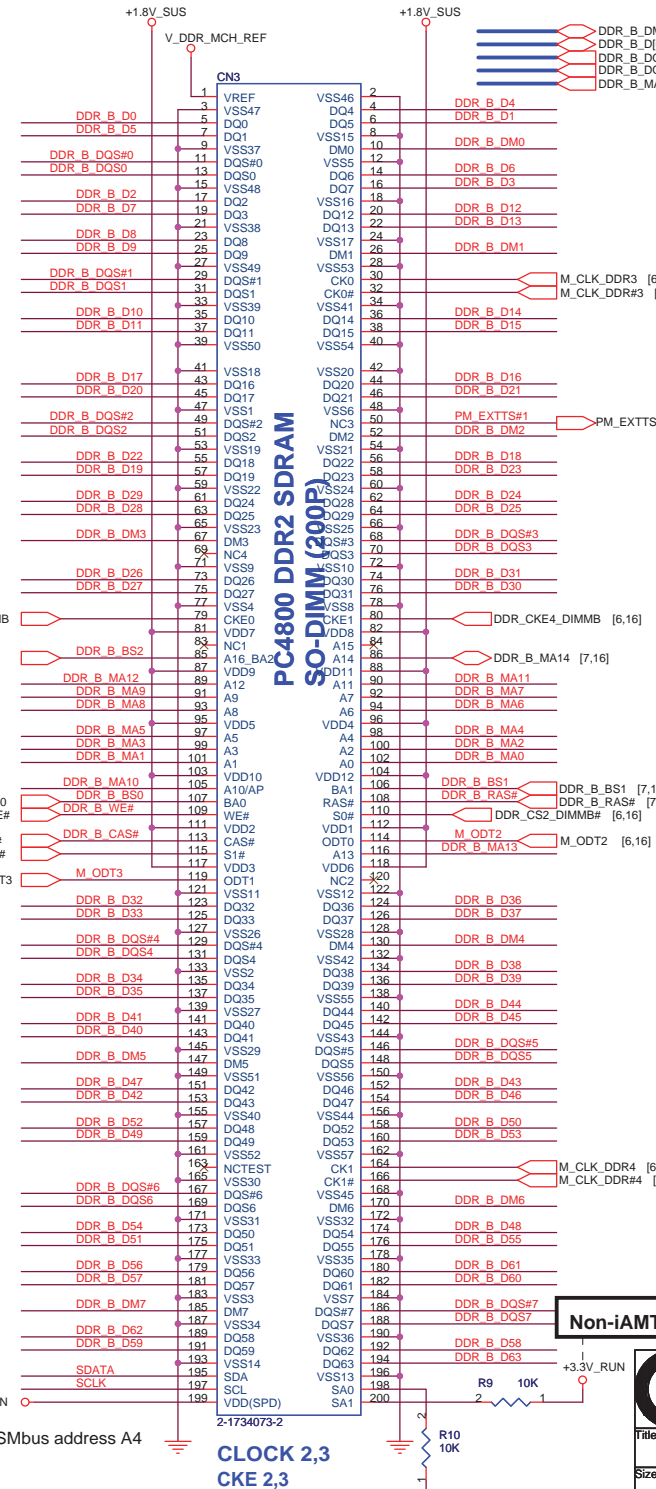
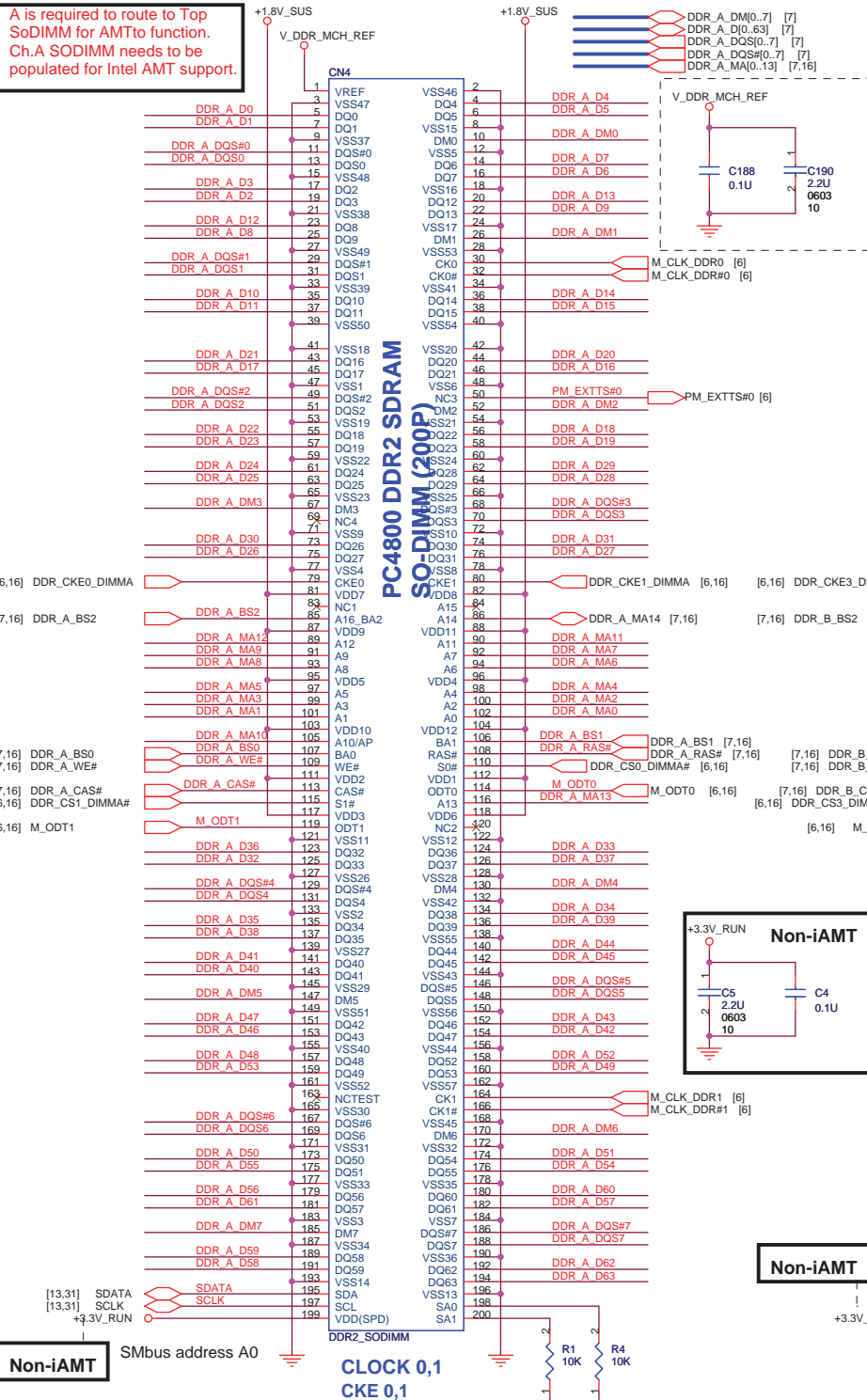
PCI-Express

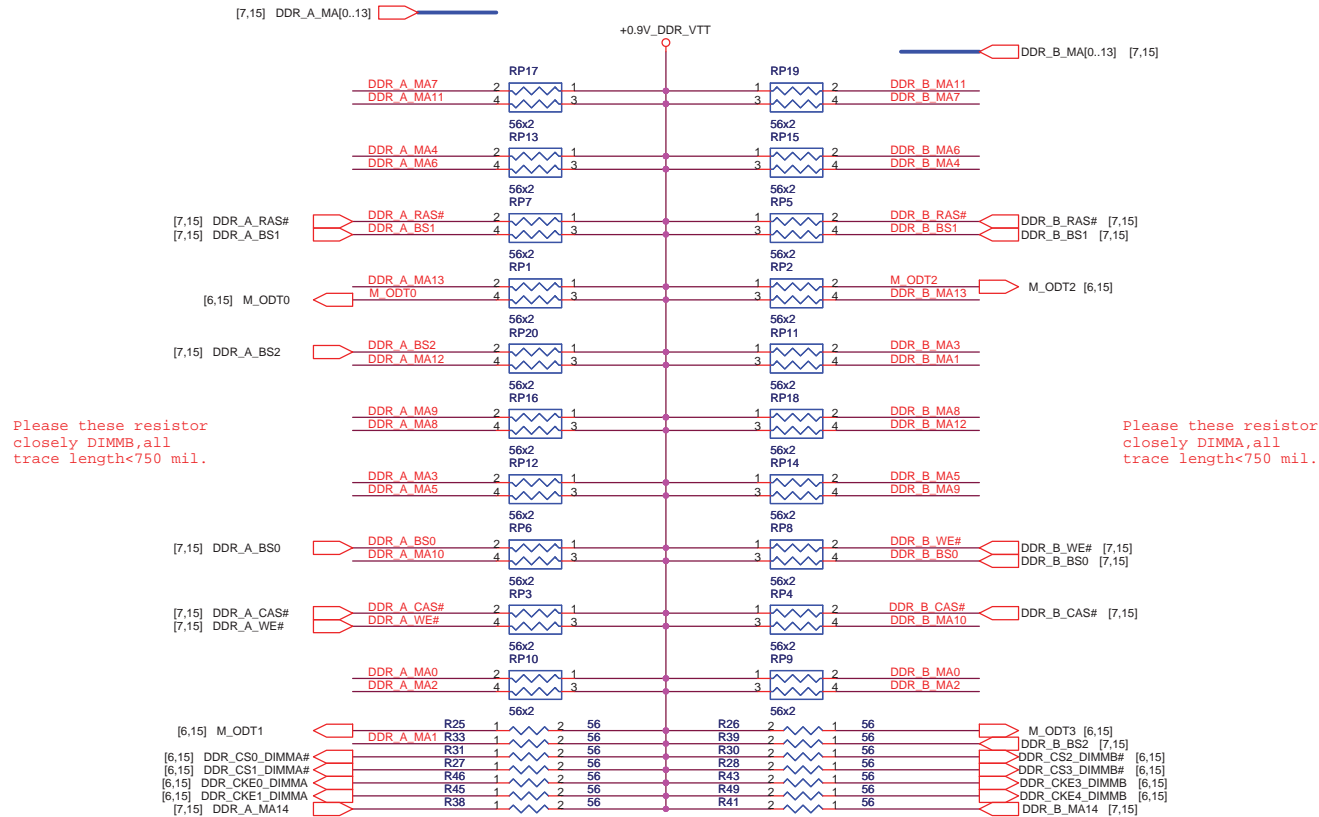
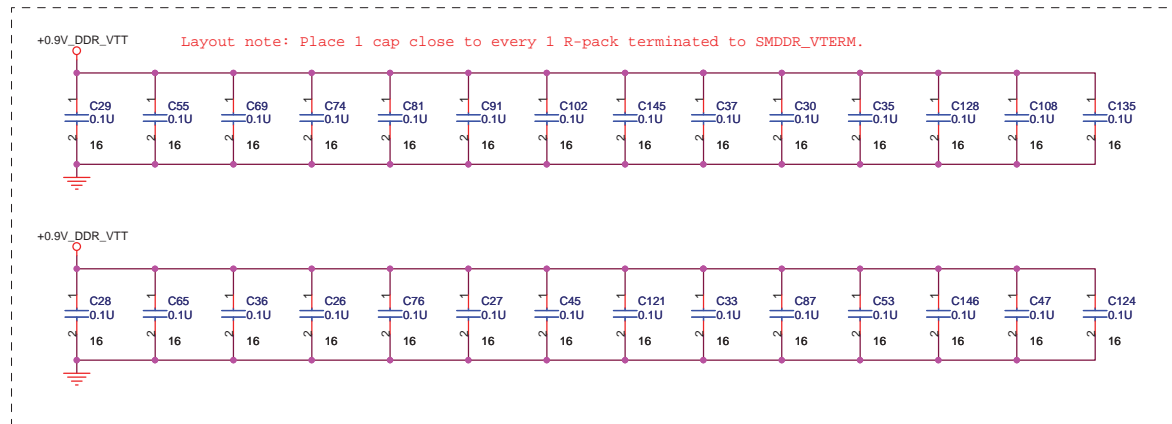
Direct Media Interface





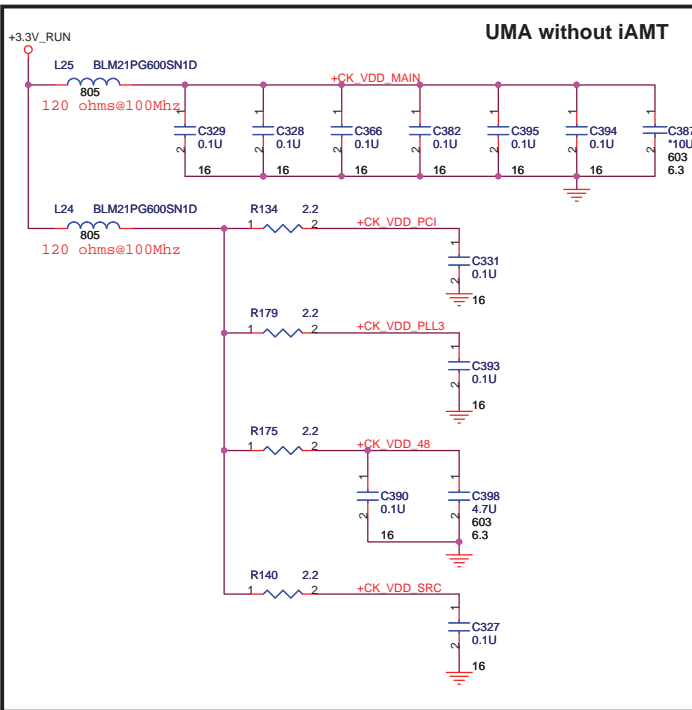
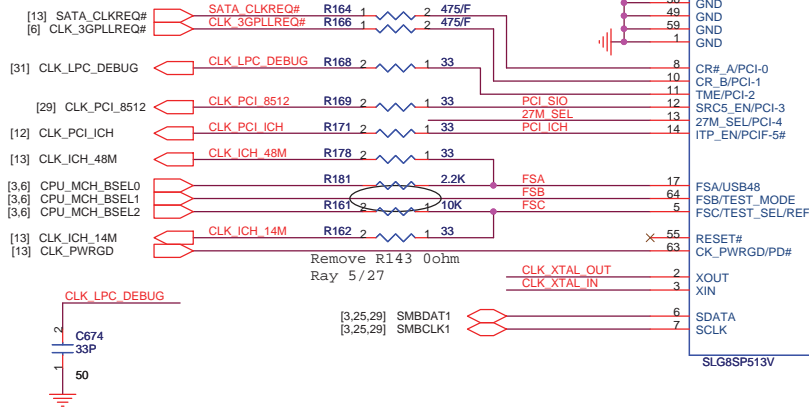
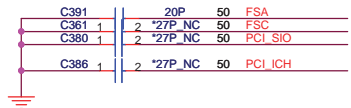
A is required to route to Top SoDIMM for AMTto function.
Ch.A SODIMM needs to be populated for Intel AMT support.





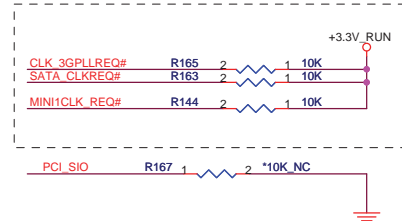
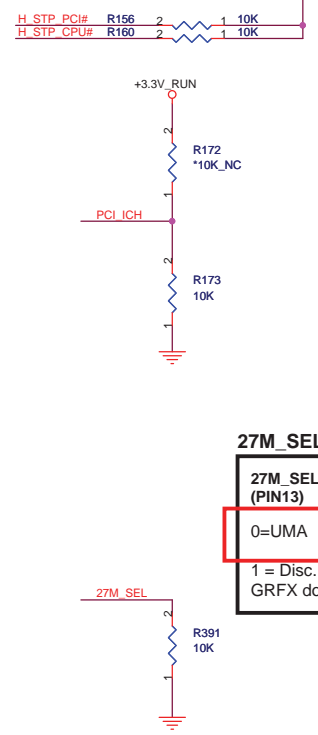
QUANTA COMPUTER	
Title: DDR2 RES ARRAY	
Size: VM8G	Rev: 1B
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Add capacitor pads for improving WWAN.



ITP_EN

PCI_ICH	10K-pull
0	Disable
1	Enable



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

QUANTA COMPUTER

File: CLOCK GENERATOR

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[6] PCIE_MTX_GRX_P[0..15]
[6] PCIE_MTX_GRX_N[0..15]

U17A
PART 1 OF 10

PCI-EXPRESS INTERFACE

PCIE_MTX_GRX_P0 AF30
PCIE_MTX_GRX_N0 AE31

PCIE_MTX_GRX_P1 AE29
PCIE_MTX_GRX_N1 AD28

PCIE_MTX_GRX_P2 AD30
PCIE_MTX_GRX_N2 AC31

PCIE_MTX_GRX_P3 AC29
PCIE_MTX_GRX_N3 AB28

PCIE_MTX_GRX_P4 AB30
PCIE_MTX_GRX_N4 AA31

PCIE_MTX_GRX_P5 AA29
PCIE_MTX_GRX_N5 Y28

PCIE_MTX_GRX_P6 Y30
PCIE_MTX_GRX_N6 W31

PCIE_MTX_GRX_P7 W29
PCIE_MTX_GRX_N7 V28

PCIE_MTX_GRX_P8 V30
PCIE_MTX_GRX_N8 U31

PCIE_MTX_GRX_P9 U29
PCIE_MTX_GRX_N9 T28

PCIE_MTX_GRX_P10 T30
PCIE_MTX_GRX_N10 R31

PCIE_MTX_GRX_P11 R29
PCIE_MTX_GRX_N11 P28

PCIE_MTX_GRX_P12 P30
PCIE_MTX_GRX_N12 N31

PCIE_MTX_GRX_P13 N29
PCIE_MTX_GRX_N13 M28

PCIE_MTX_GRX_P14 M30
PCIE_MTX_GRX_N14 L31

PCIE_MTX_GRX_P15 L29
PCIE_MTX_GRX_N15 K30

PCIE_RX0P
PCIE_RX0N

PCIE_RX1P
PCIE_RX1N

PCIE_RX2P
PCIE_RX2N

PCIE_RX3P
PCIE_RX3N

PCIE_RX4P
PCIE_RX4N

PCIE_RX5P
PCIE_RX5N

PCIE_RX6P
PCIE_RX6N

PCIE_RX7P
PCIE_RX7N

PCIE_RX8P
PCIE_RX8N

PCIE_RX9P
PCIE_RX9N

PCIE_RX10P
PCIE_RX10N

PCIE_RX11P
PCIE_RX11N

PCIE_RX12P
PCIE_RX12N

PCIE_RX13P
PCIE_RX13N

PCIE_RX14P
PCIE_RX14N

PCIE_RX15P
PCIE_RX15N

PCIE_TX0P
PCIE_TX0N

PCIE_TX1P
PCIE_TX1N

PCIE_TX2P
PCIE_TX2N

PCIE_TX3P
PCIE_TX3N

PCIE_TX4P
PCIE_TX4N

PCIE_TX5P
PCIE_TX5N

PCIE_TX6P
PCIE_TX6N

PCIE_TX7P
PCIE_TX7N

PCIE_TX8P
PCIE_TX8N

PCIE_TX9P
PCIE_TX9N

PCIE_TX10P
PCIE_TX10N

PCIE_TX11P
PCIE_TX11N

PCIE_TX12P
PCIE_TX12N

PCIE_TX13P
PCIE_TX13N

PCIE_TX14P
PCIE_TX14N

PCIE_TX15P
PCIE_TX15N

PCIE_MRX_GTX_C_P0 AH30
PCIE_MRX_GTX_C_N0 AG31

PCIE_MRX_GTX_C_P1 AG29
PCIE_MRX_GTX_C_N1 AF28

PCIE_MRX_GTX_C_P2 AF27
PCIE_MRX_GTX_C_N2 AF26

PCIE_MRX_GTX_C_P3 AD27
PCIE_MRX_GTX_C_N3 AD26

PCIE_MRX_GTX_C_P4 AC25
PCIE_MRX_GTX_C_N4 AB25

PCIE_MRX_GTX_C_P5 Y23
PCIE_MRX_GTX_C_N5 Y24

PCIE_MRX_GTX_C_P6 AB27
PCIE_MRX_GTX_C_N6 AB26

PCIE_MRX_GTX_C_P7 Y27
PCIE_MRX_GTX_C_N7 Y26

PCIE_MRX_GTX_C_P8 W24
PCIE_MRX_GTX_C_N8 W23

PCIE_MRX_GTX_C_P9 V27
PCIE_MRX_GTX_C_N9 U26

PCIE_MRX_GTX_C_P10 U24
PCIE_MRX_GTX_C_N10 U23

PCIE_MRX_GTX_C_P11 T26
PCIE_MRX_GTX_C_N11 T27

PCIE_MRX_GTX_C_P12 T24
PCIE_MRX_GTX_C_N12 T23

PCIE_MRX_GTX_C_P13 P27
PCIE_MRX_GTX_C_N13 P26

PCIE_MRX_GTX_C_P14 P24
PCIE_MRX_GTX_C_N14 P23

PCIE_MRX_GTX_C_P15 M27
PCIE_MRX_GTX_C_N15 N26

[6] PCIE_MRX_GTX_P[0..15]
[6] PCIE_MRX_GTX_N[0..15]

PCIE_MRX_GTX_P0 0.1U 2 1 C350 16 PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1 0.1U 2 1 C345 16 PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2 0.1U 2 1 C342 16 PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3 0.1U 2 1 C347 16 PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4 0.1U 2 1 C349 16 PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5 0.1U 2 1 C376 16 PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6 0.1U 2 1 C357 16 PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7 0.1U 2 1 C373 16 PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8 0.1U 2 1 C355 16 PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9 0.1U 2 1 C353 16 PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10 0.1U 2 1 C340 16 PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11 0.1U 2 1 C372 16 PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12 0.1U 2 1 C338 16 PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13 0.1U 2 1 C370 16 PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14 0.1U 2 1 C364 16 PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15 0.1U 2 1 C560 16 PCIE_MRX_GTX_C_P15

PCIE_MRX_GTX_N0 0.1U 2 1 C351 16 PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1 0.1U 2 1 C344 16 PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2 0.1U 2 1 C343 16 PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3 0.1U 2 1 C346 16 PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4 0.1U 2 1 C348 16 PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5 0.1U 2 1 C375 16 PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6 0.1U 2 1 C356 16 PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7 0.1U 2 1 C374 16 PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8 0.1U 2 1 C354 16 PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9 0.1U 2 1 C352 16 PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10 0.1U 2 1 C339 16 PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11 0.1U 2 1 C371 16 PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12 0.1U 2 1 C337 16 PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13 0.1U 2 1 C369 16 PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14 0.1U 2 1 C363 16 PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15 0.1U 2 1 C561 16 PCIE_MRX_GTX_C_N15

100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
clock must be provided less than 400ns
after CLKREQ# is asserted


[17] CLK_PCIE_VGA AK30
[17] CLK_PCIE_VGA# AK32

[13] PLTRST_DELAY# R155 1 2 AL27
[6,12,28,29,31,38,39] PLTRST#

Remove R158 0ohm
Ray 5/27

PCIE_CALRN AA22 PCIE_CALRN 2.0K R149
PCIE_CALRP Y22 PCIE_CALRP 1.27K R119

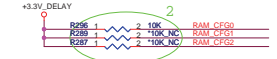
(1.1V)
+PCIE_VDDC



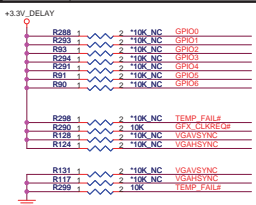
**QUANTA
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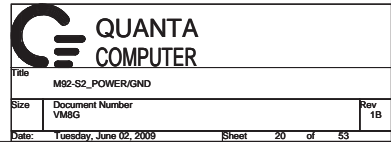
Title M92-S2_PCIE		
Size VM8G	Document Number	Rev 1B
Date: Tuesday, June 02, 2009	Sheet 18	of 53

MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG1 GP109	CFG2 GP1013	CFG3 GP1012	CFG0 GP1011
128MB	0	0	0	0
256MB	0	0	0	1
64MB	0	1	1	0
512MB	1	0	0	0

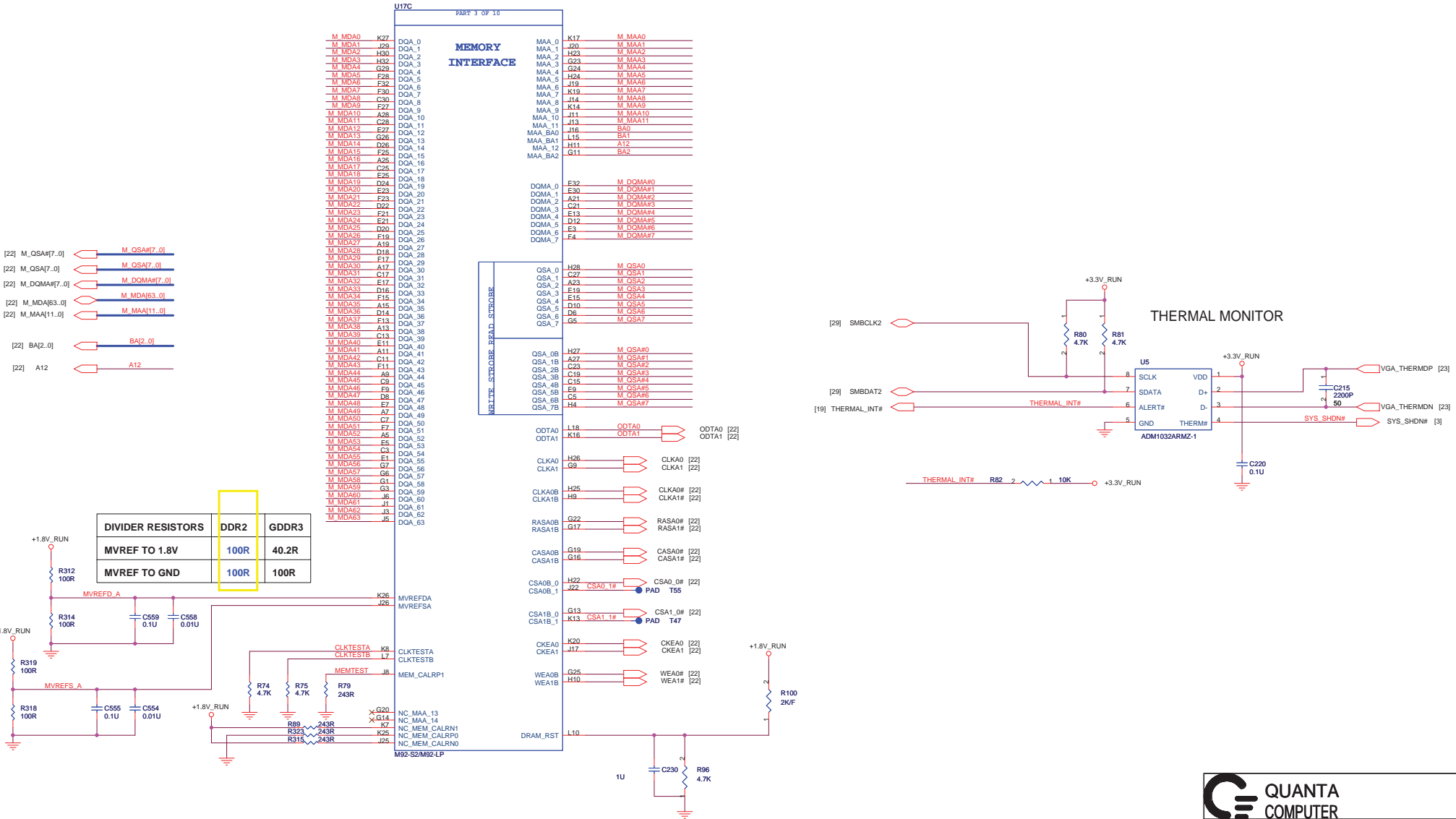


GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	FBs setting
GPIO0	GPIO0(-) TX_PWR5_ENB (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO1(-) TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO2(-) RIF_GEN2_EN (5.0 GT/s Enable) 0: Default (Driver Controlled Gen2) 1: Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO 5, AC, BATT 0: Battery saving mode = 0.0 V 1: AC (Performance mode) = 3.3 V	0
GPIO6	ATI Internal use only	0





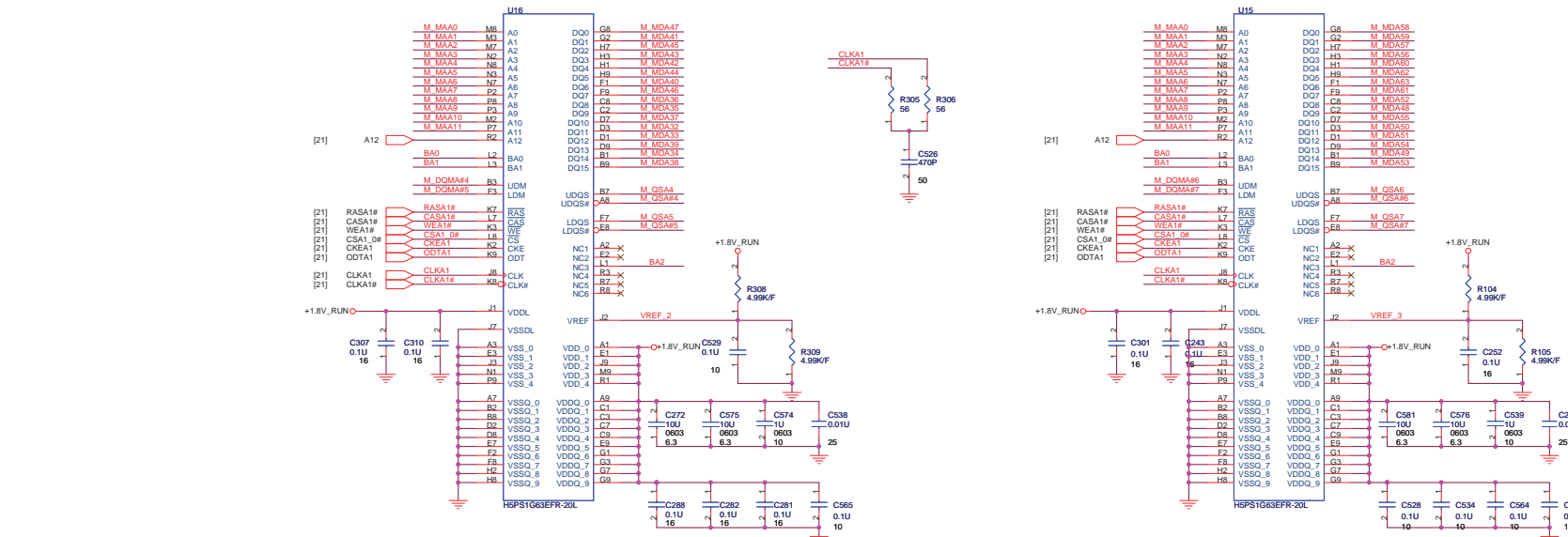
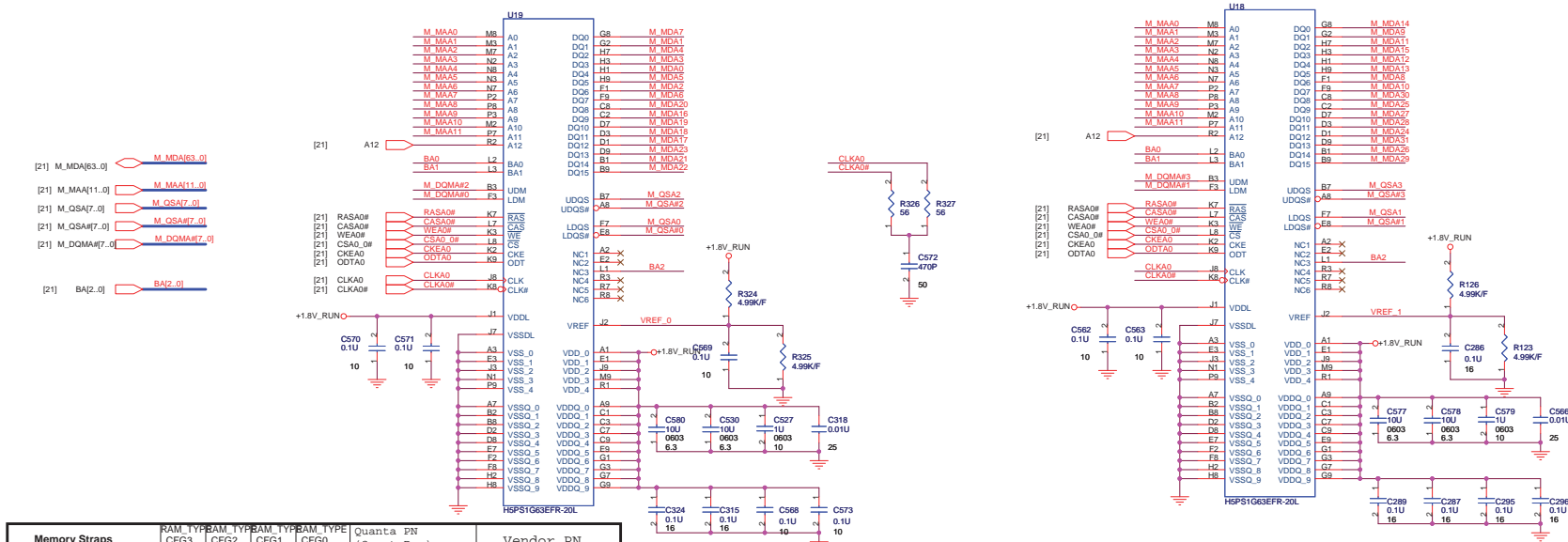
MEMORY INTERFACE



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COMPUTER

Title: MEMORY/THERM
Size: Document Number: VM8G
Date: Tuesday, June 02, 2009 Sheet: 21 of 53

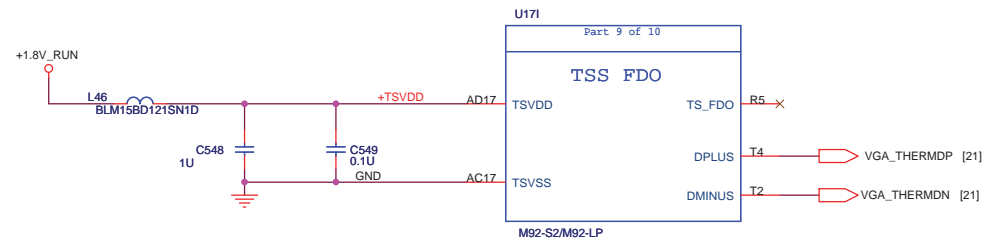
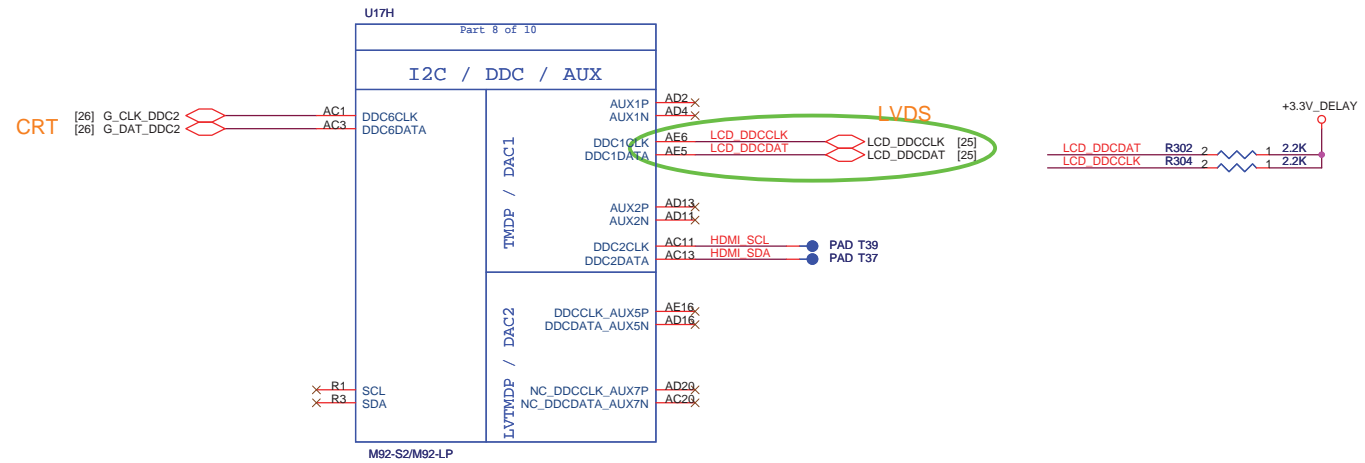
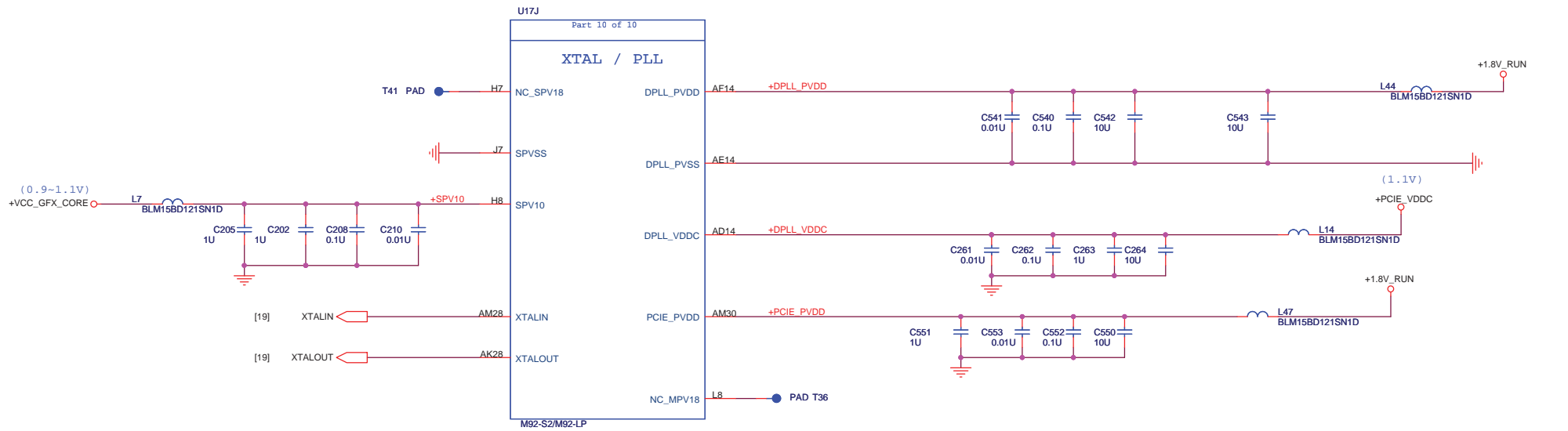
DDR2 64MbitX16 MEMORY




QUANTA

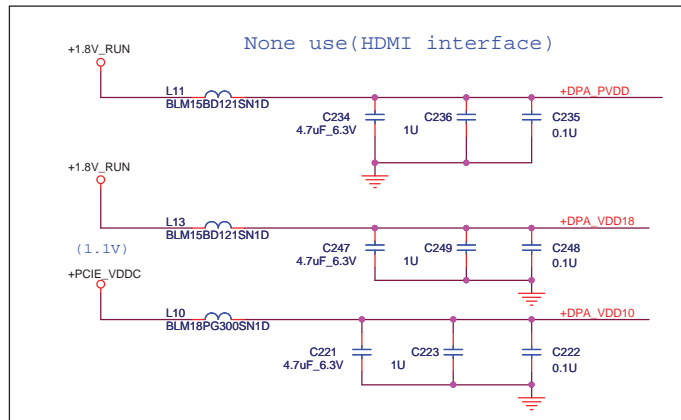
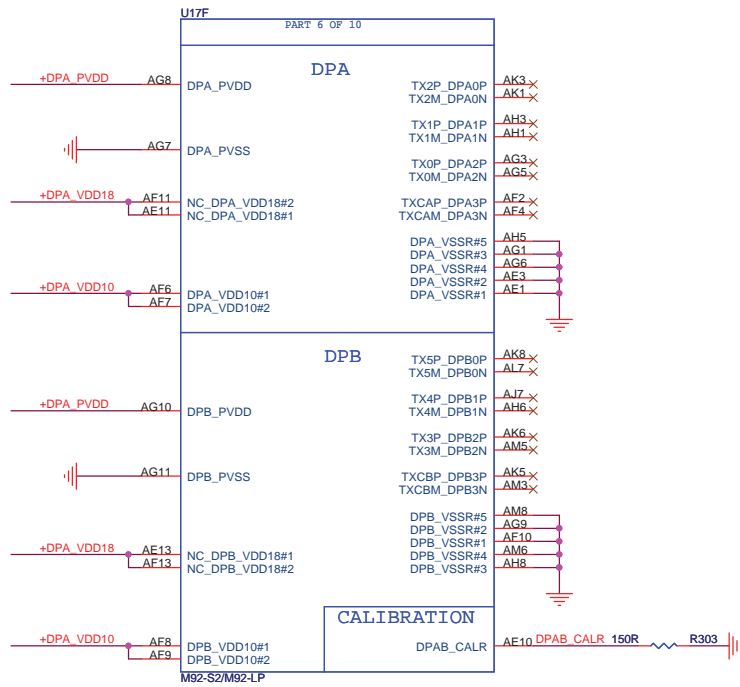
COMPUTER

File: MS2-S2_DDR2_512M		
Size	Document Number: VMBC	Rev: 1B
Date: Saturday, June 06, 2009		Sheet: 22 of 33

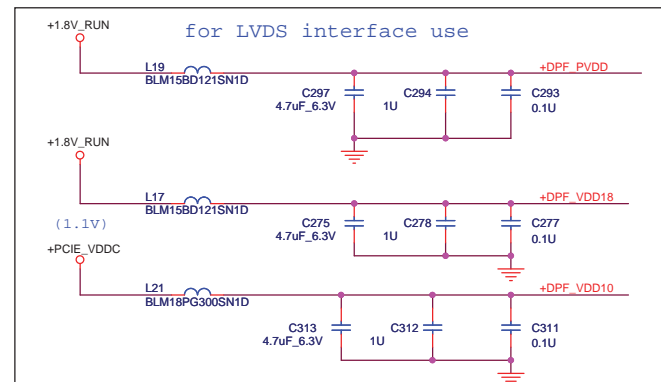
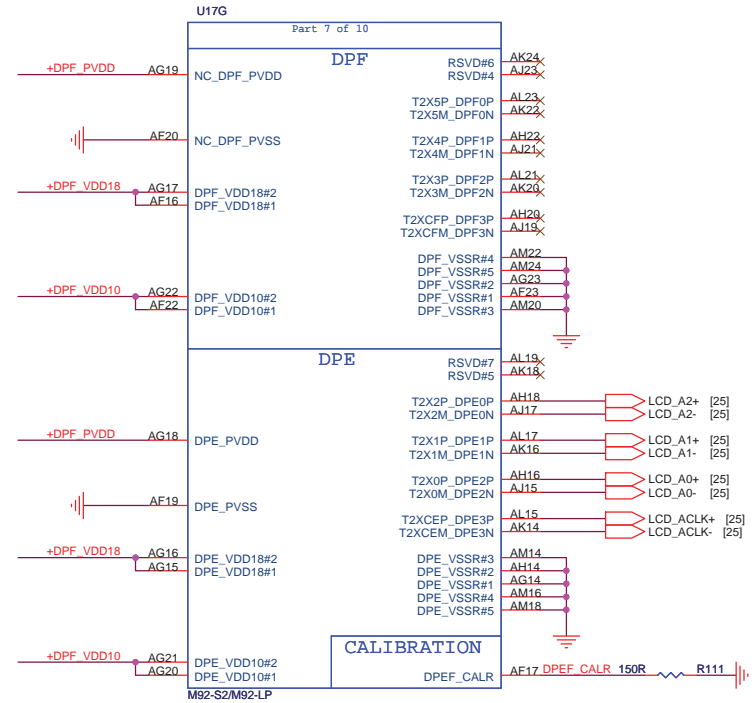


 QUANTA COMPUTER			
File	M92-S2_XTAL/PLL/I2C		
Size	Document Number	Rev	
VM8G		1B	
Date:	Tuesday, June 02, 2009	Sheet	23 of 53

TMDP(HDMI) INTERFACE

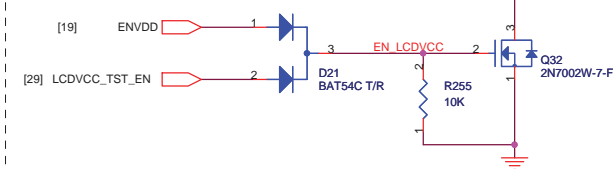


LVDS INTERFACE

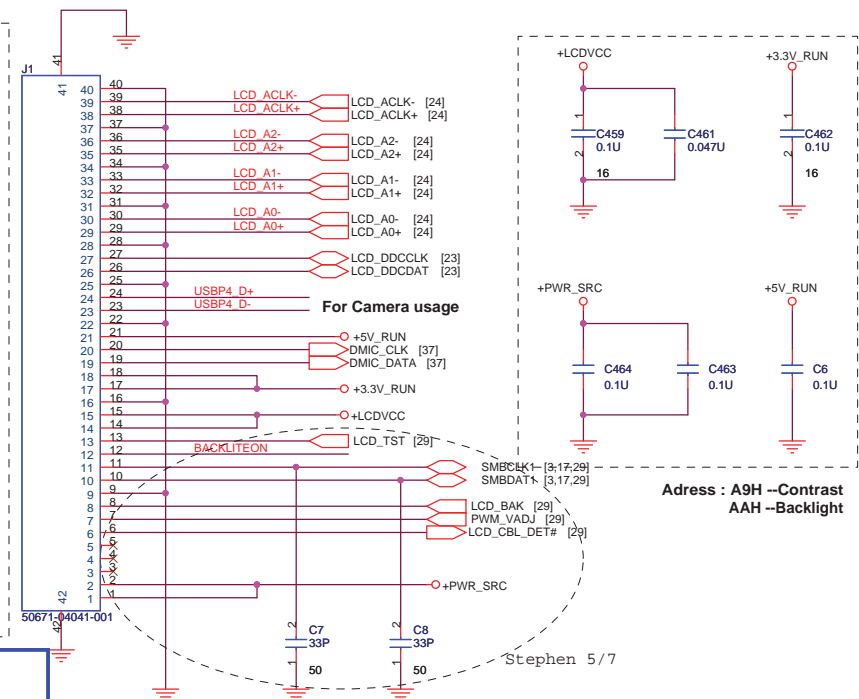
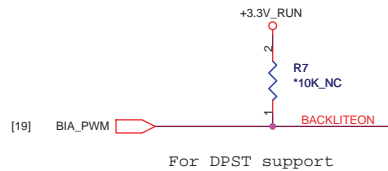
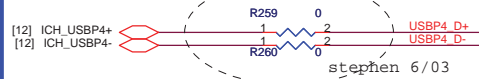


File	M92-S2_TMDP I/F	Rev	1B
Size	Document Number VM8G		
Date:	Tuesday, June 02, 2009	Sheet	24 of 53

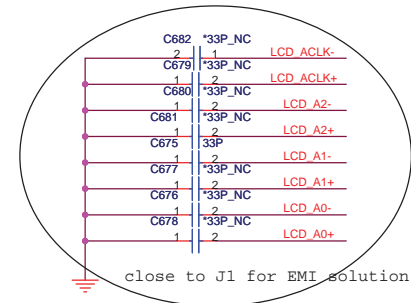
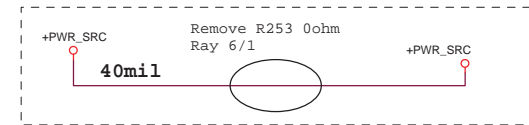
Support the new imbedded diagnostics.



Camera support



Address : A9H --Contrast
AAH --Backlight



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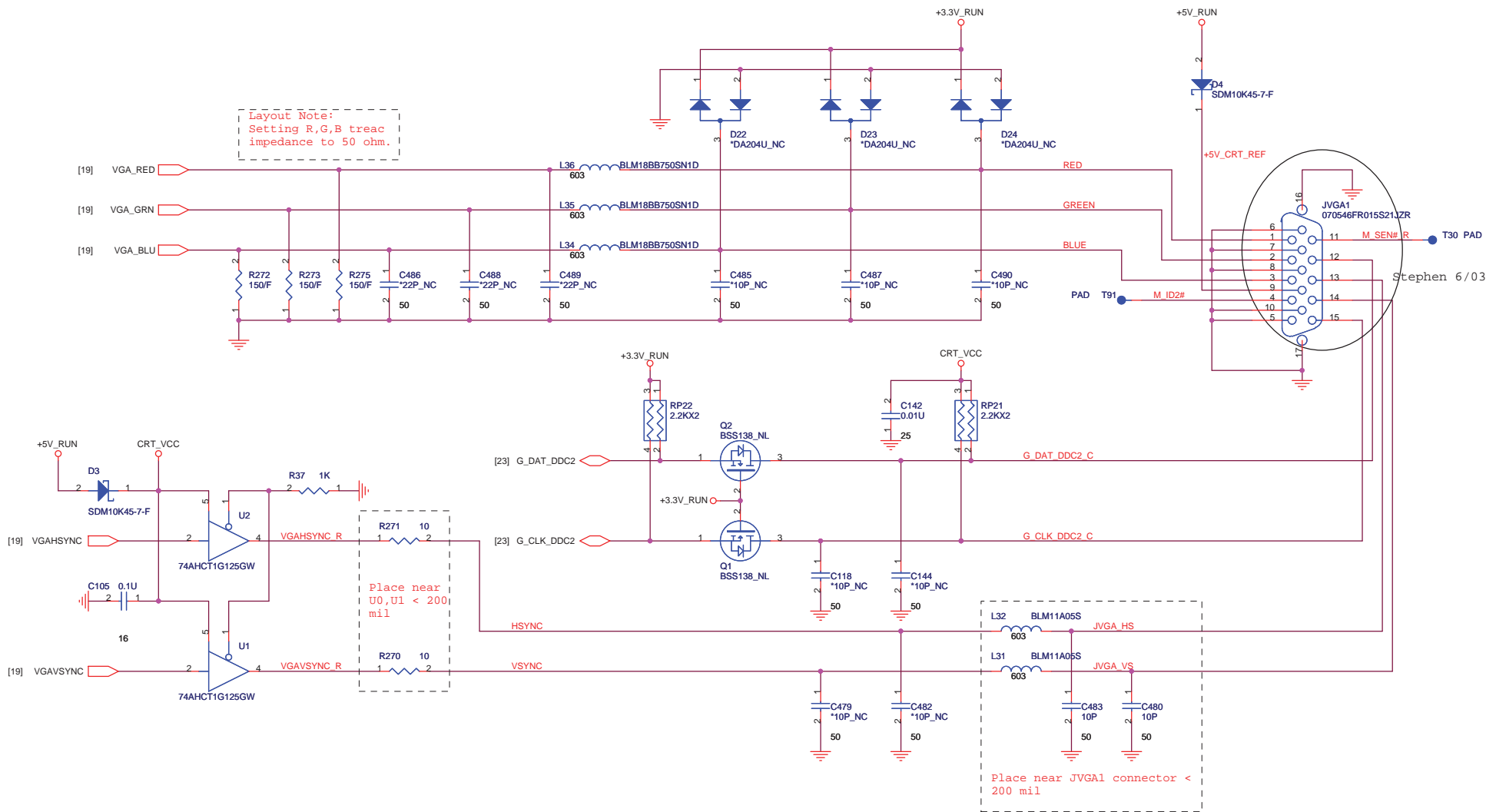
File: LCD CONN & CK-SSCD


Size: Document Number VM8G

Date: Wednesday, June 03, 2009

Rev 1B

Sheet 25 of 53




 QUANTA COMPUTER			
File	CRT&TV CONN		
Size	Document Number	Rev	
	VM8G	1B	
Date:	Wednesday, June 03, 2009	Sheet	26 of 53

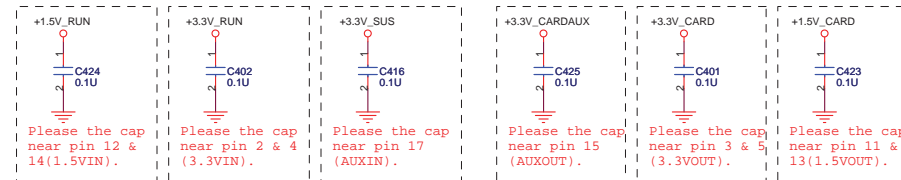
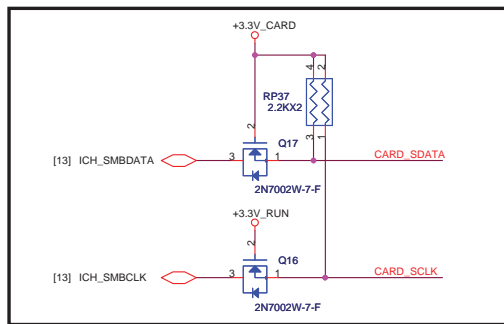
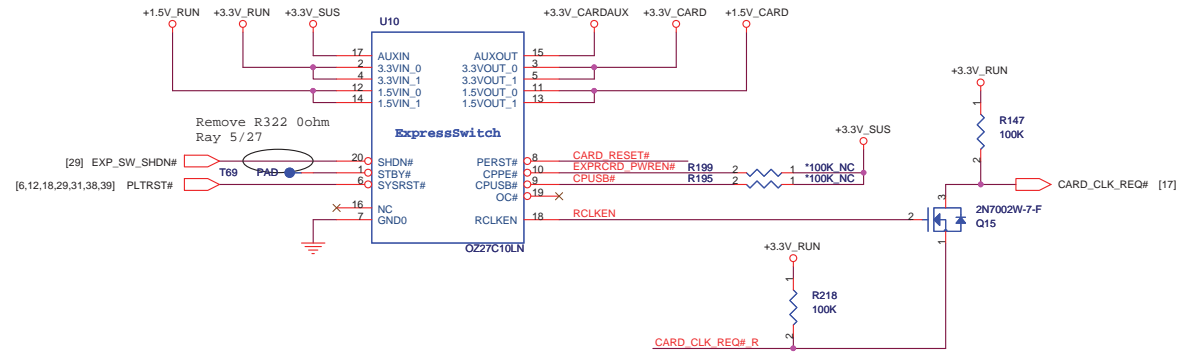
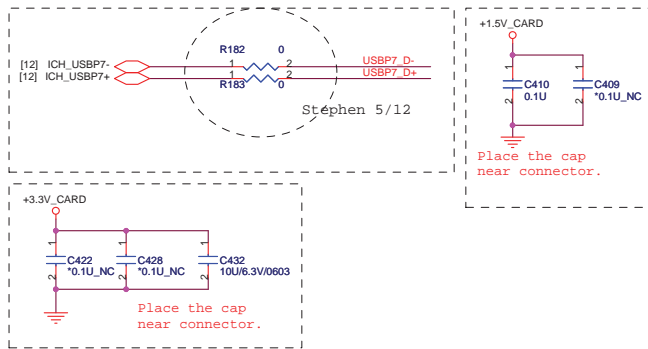


<http://laptop-motherboard-schematic.blogspot.com/>

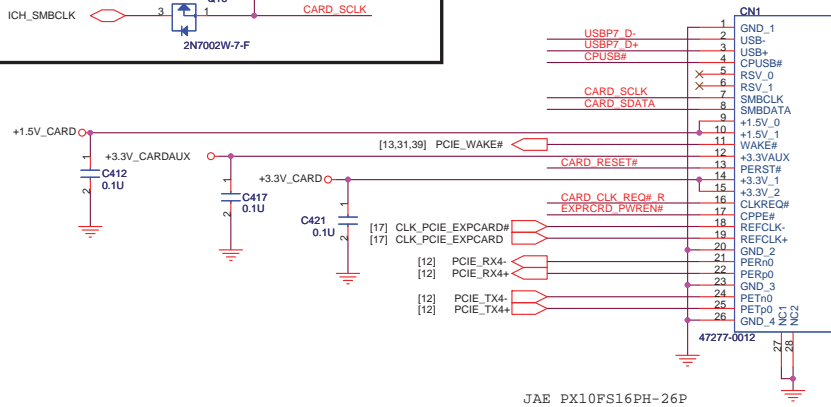
www.vinafix.vn

		QUANTA COMPUTER	
Title Card Reader-RTS5158E			
Size	Document Number VM8G		Rev 1B
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+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

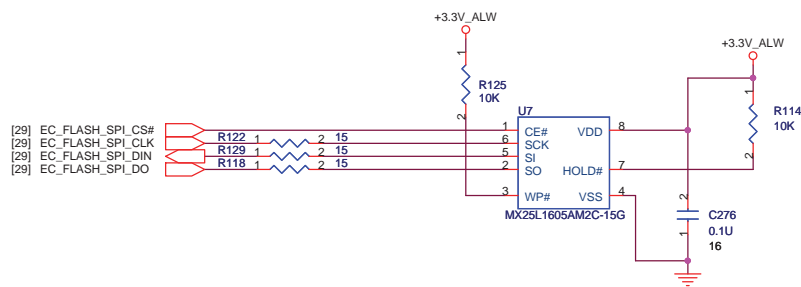


Express Card

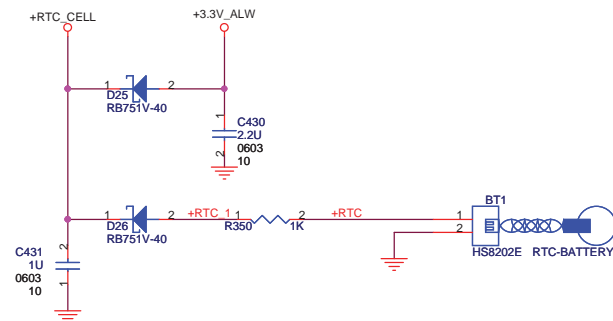


*Express Card cage

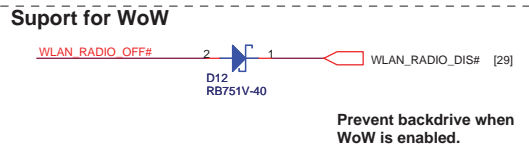
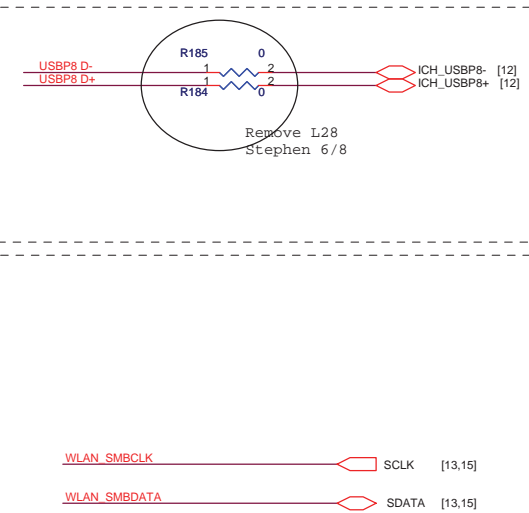
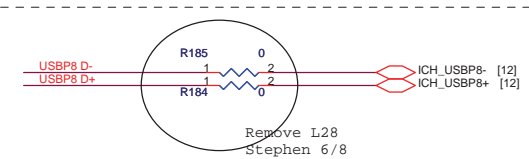
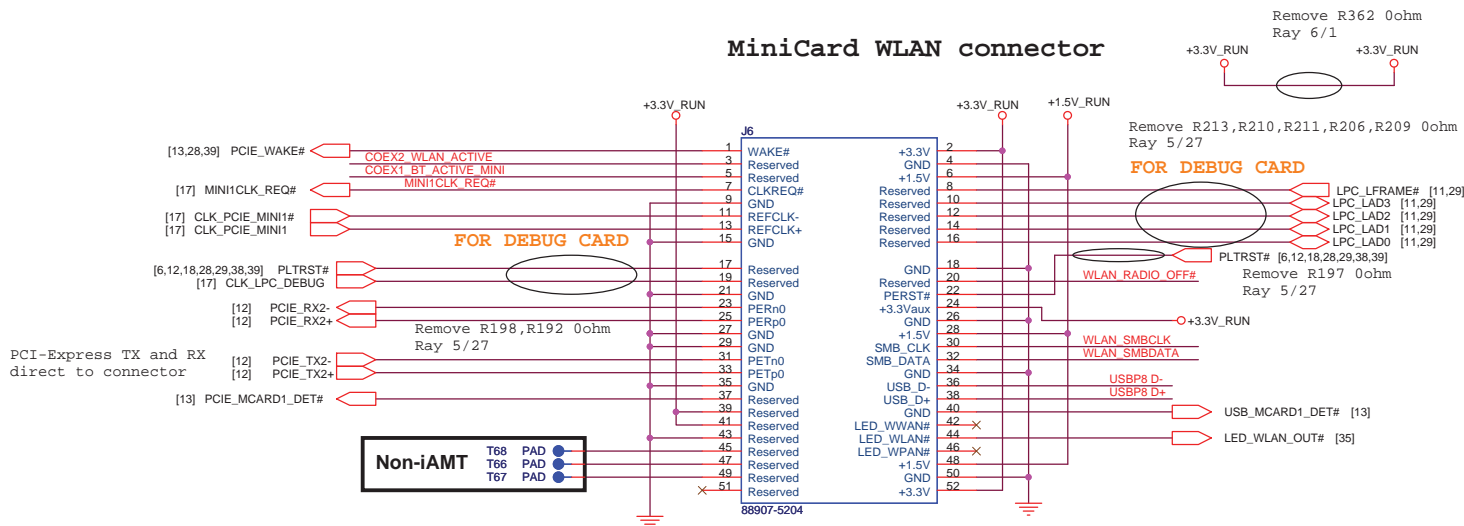
16Mbit (2M Byte), SPI



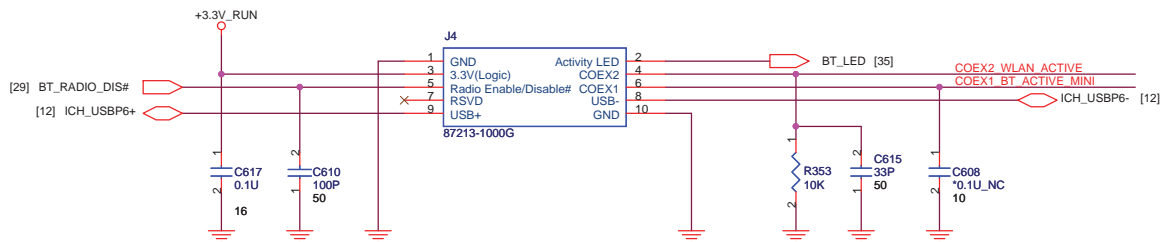
RTC BATTERY



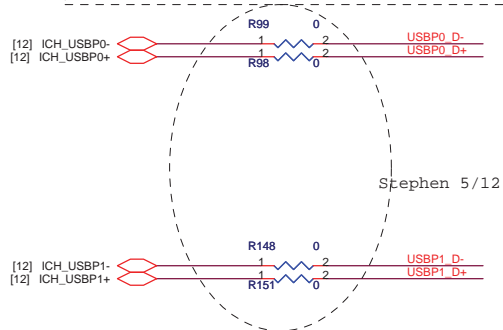
MiniCard WLAN connector



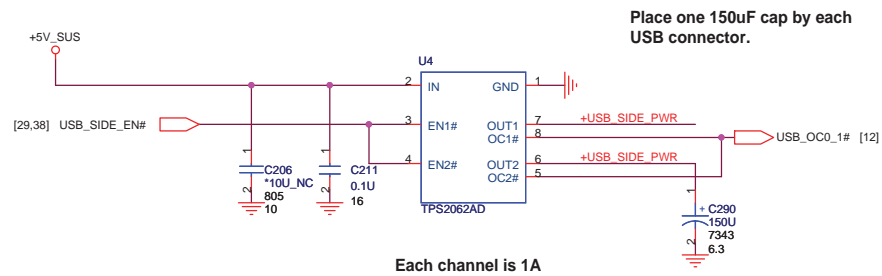
Bluetooth



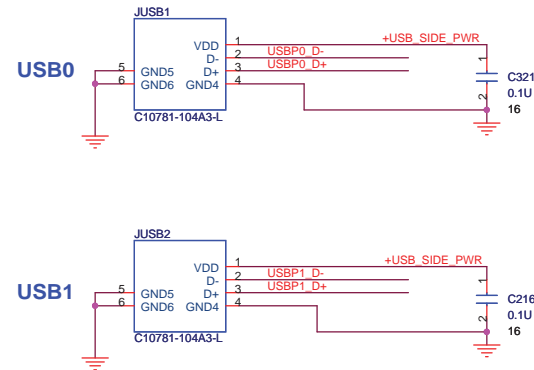
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



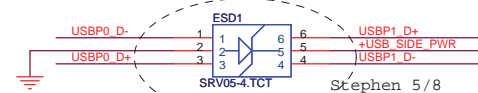
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



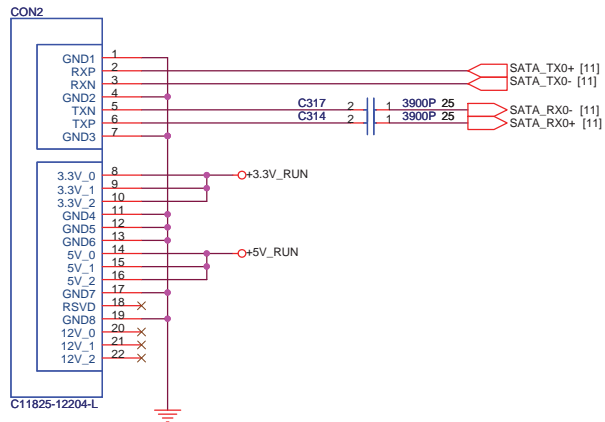
Place one 150uF cap by each USB connector.



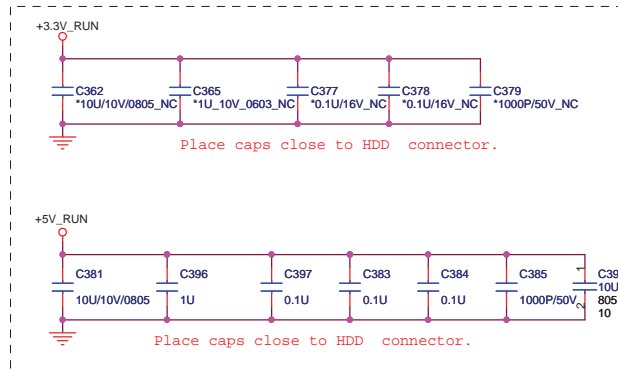
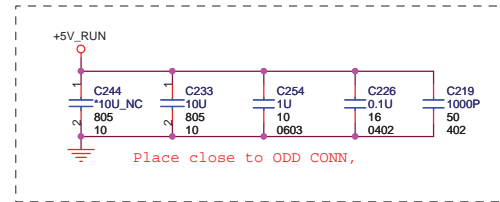
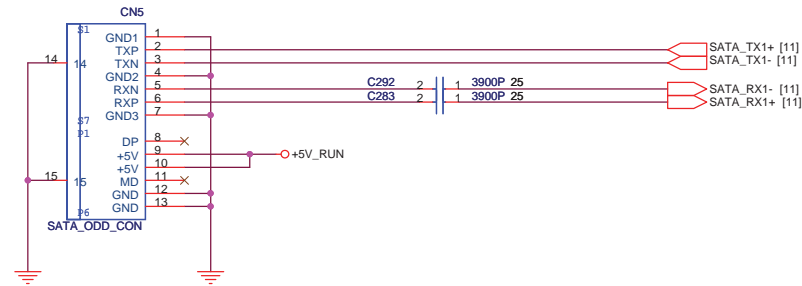
Place ESD diodes as close as USB connector.



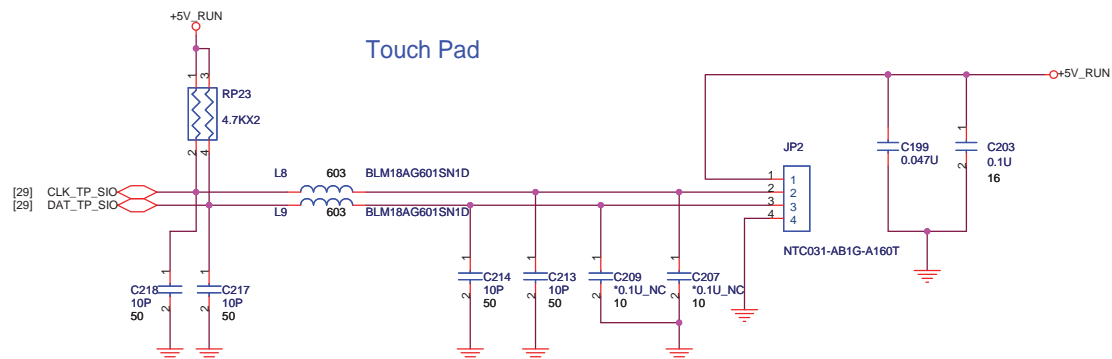
SATA HDD Connector.



SATA ODD Connector.



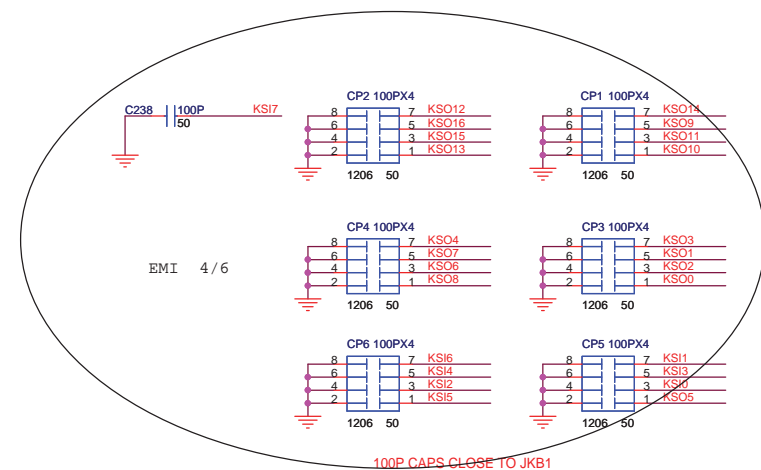
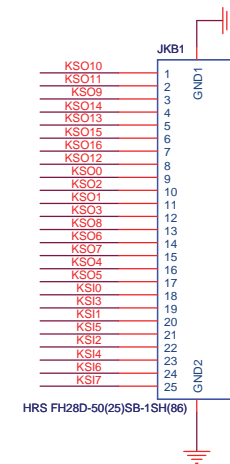
Touch Pad



KEYBOARD CONNECTOR

[29] KSO[0..16]

[29] KSI[0..7]

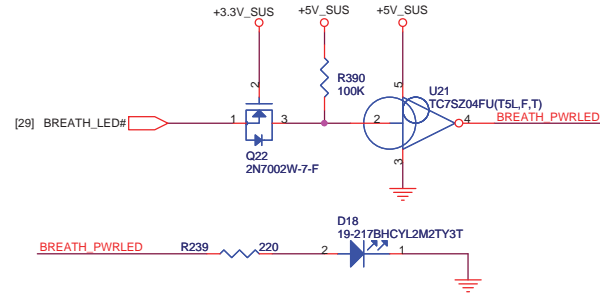


Keyboard LED

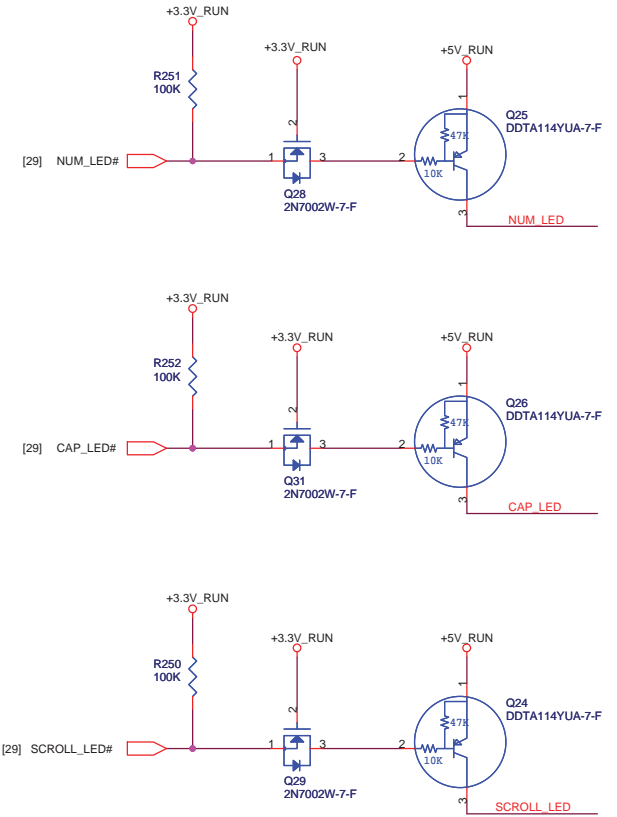
Dash board connector



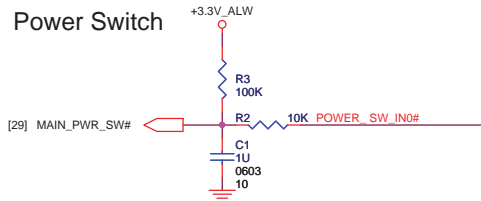
Power & Suspend.



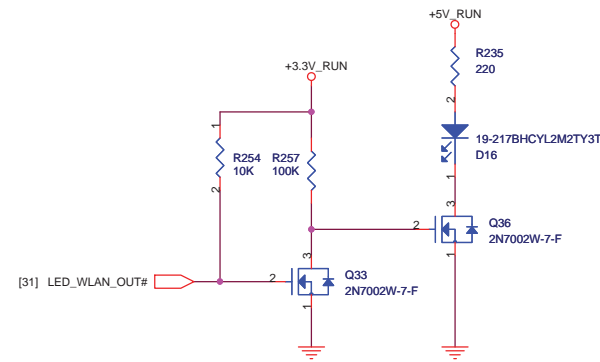
Keyboard LED



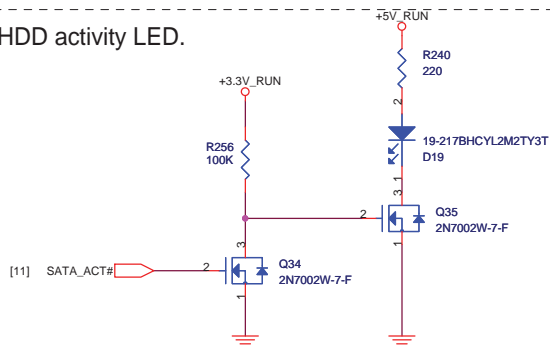
Power Switch



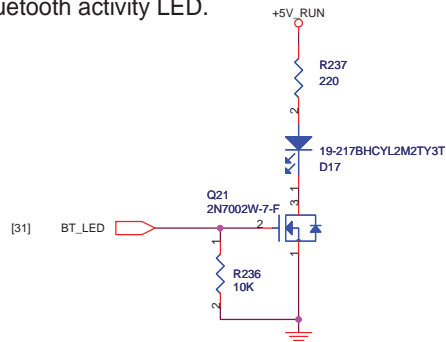
WLAN



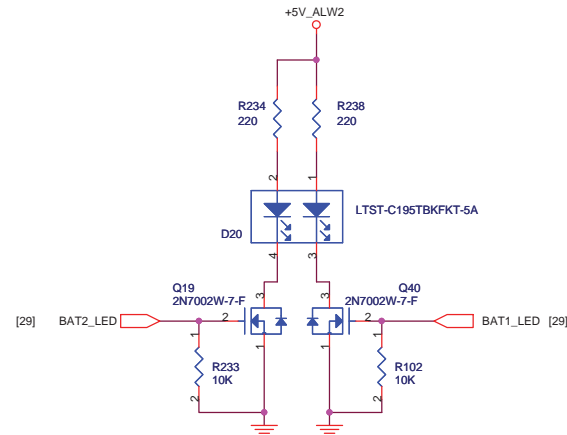
HDD activity LED.

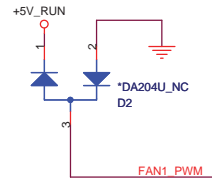
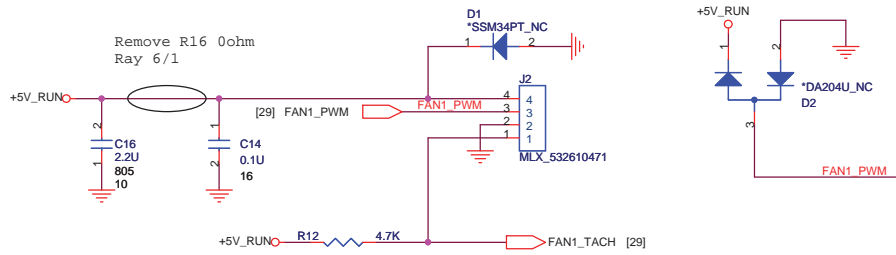



Bluetooth activity LED.

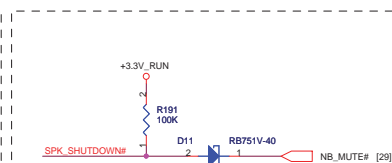


Battery status.



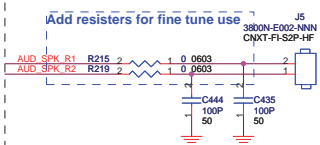


 QUANTA COMPUTER			
Title FAN & THERMAL			
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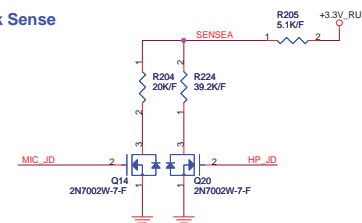


Add PC beep for system error circuit No9 10.14
Del PC beep No9 10.15

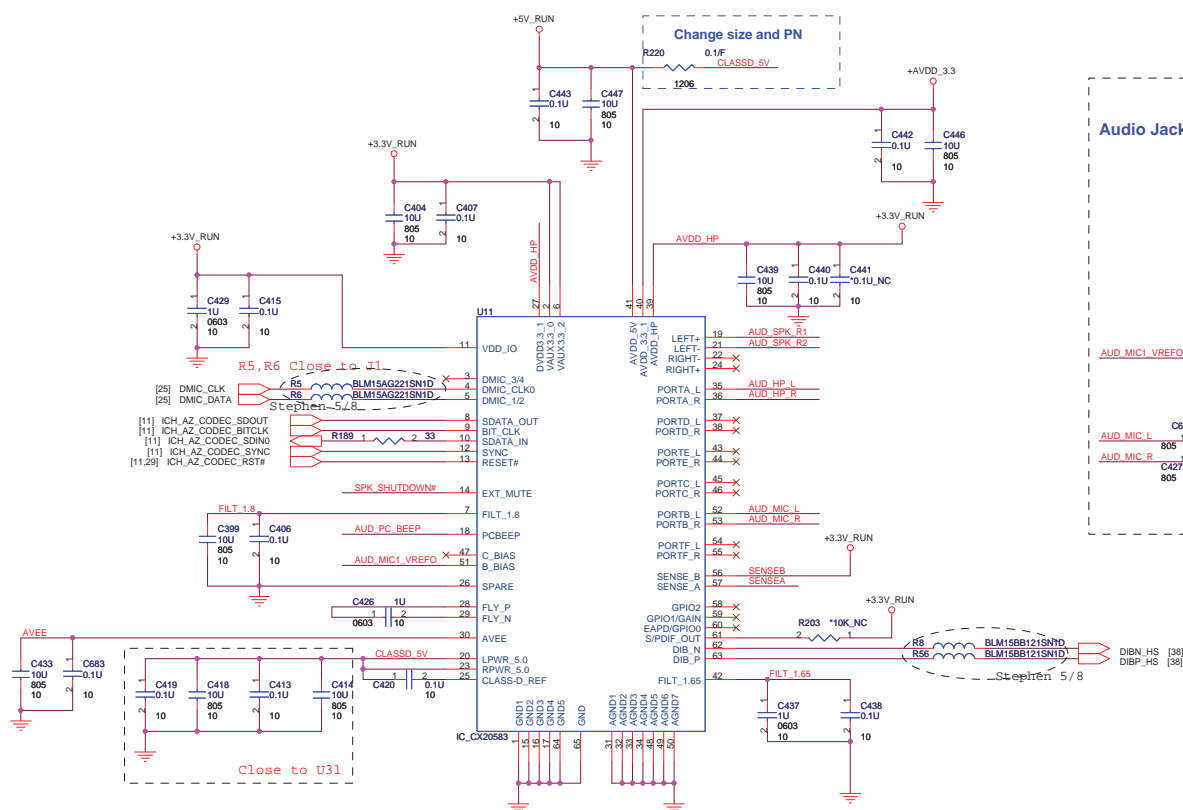
Speakers conn



Jack Sense



AUDIO CODEC



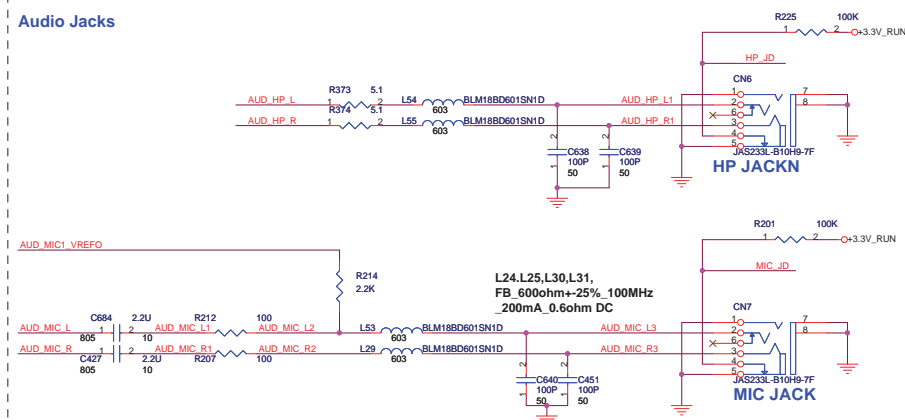
PC BEEP

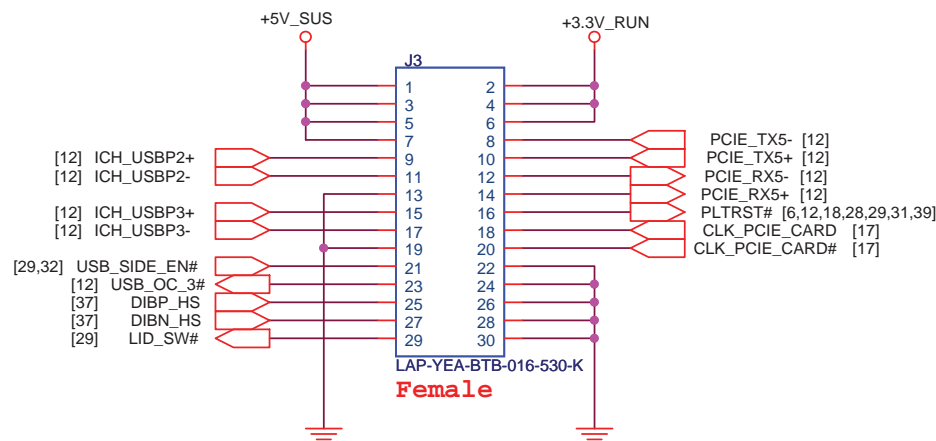
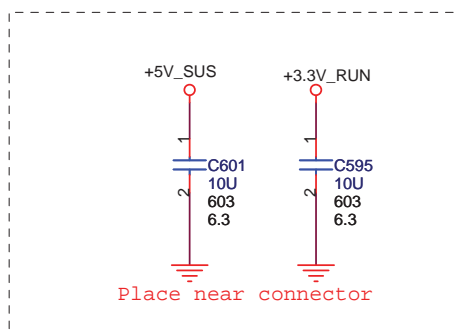
Close to U1




Change Beep design

Audio Jacks






Board to board connector (Modem Card + Cardreader+1394a+ 2 USB Port)

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		QUANTA COMPUTER	
Title System Reset Circuit			
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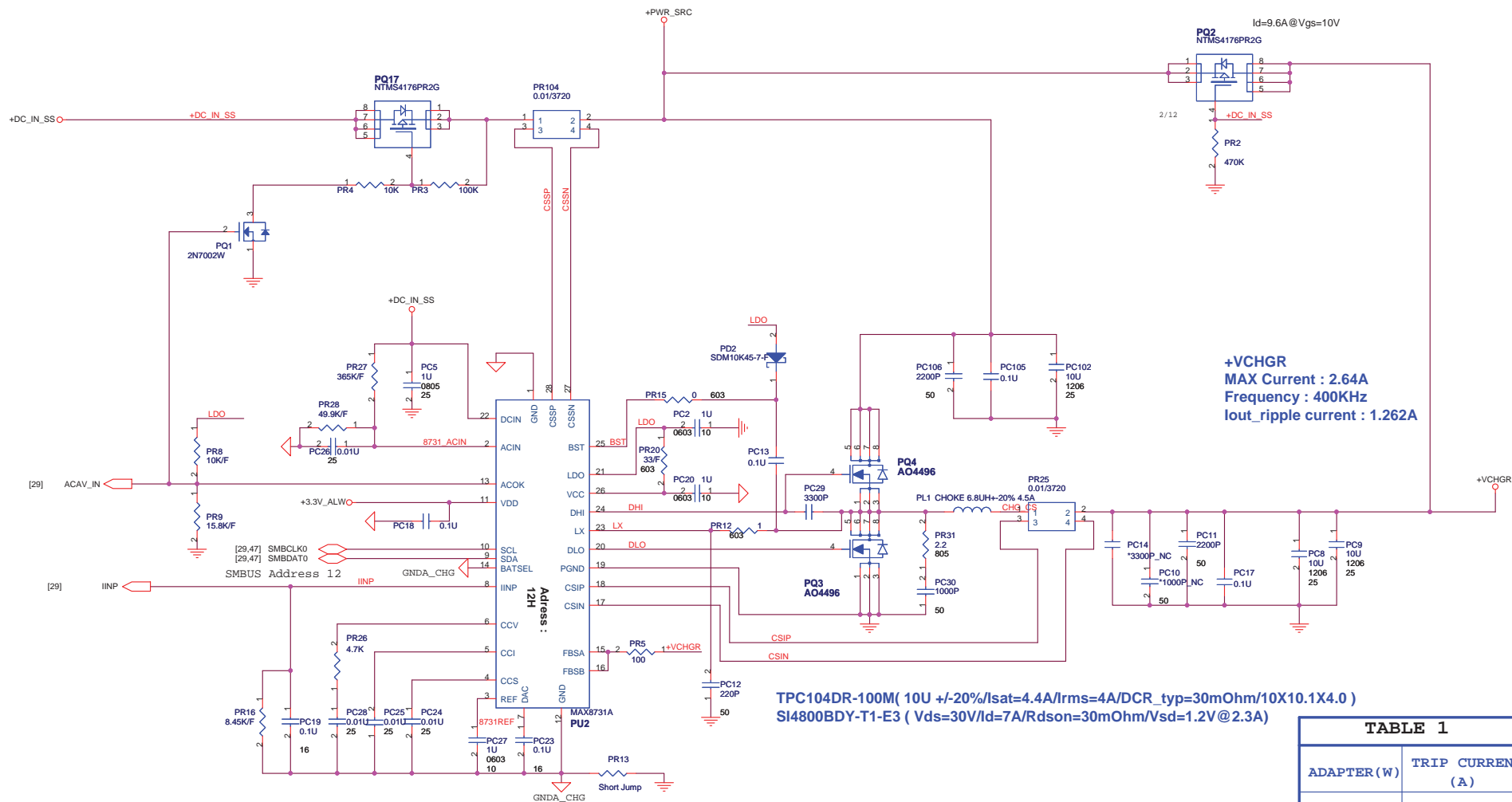


TABLE 1

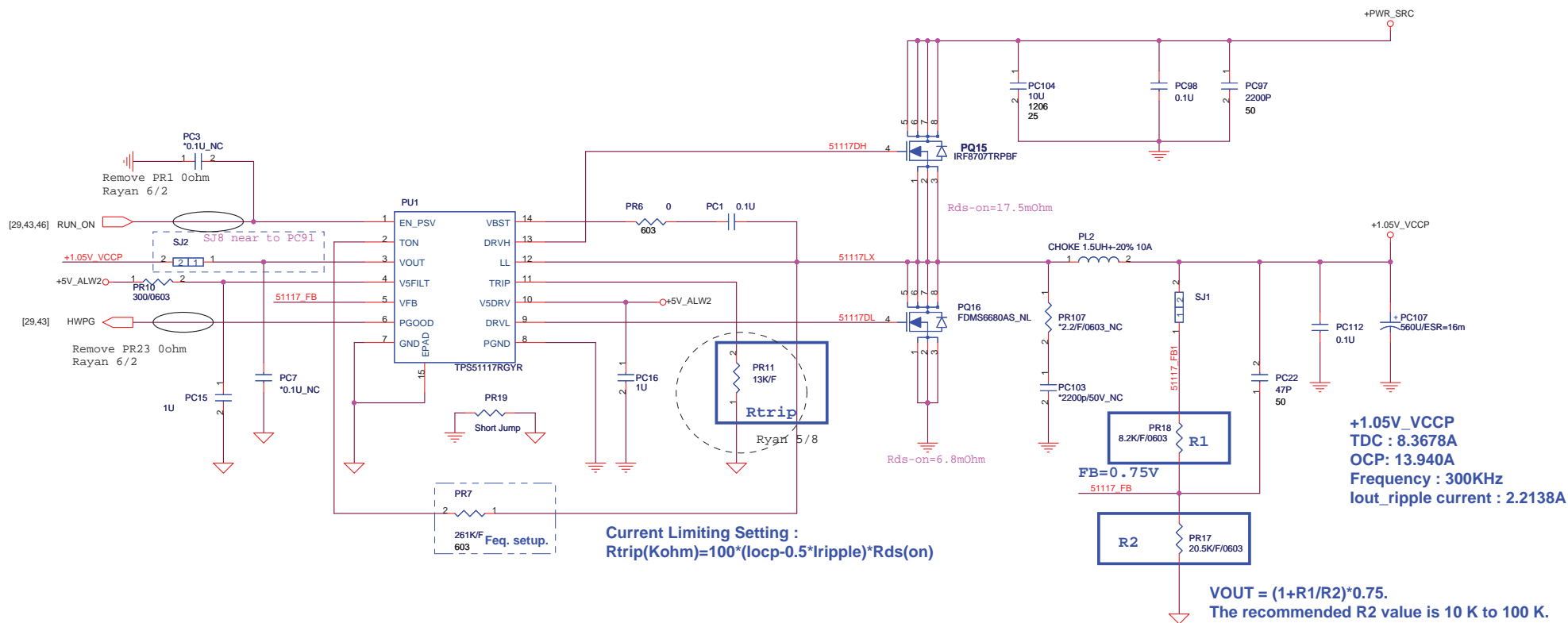
ADAPTER(W)	TRIP CURRENT (A)
65	3.17
90	4.43
130	6.43
150	7.43
200	9.75
230	11.28



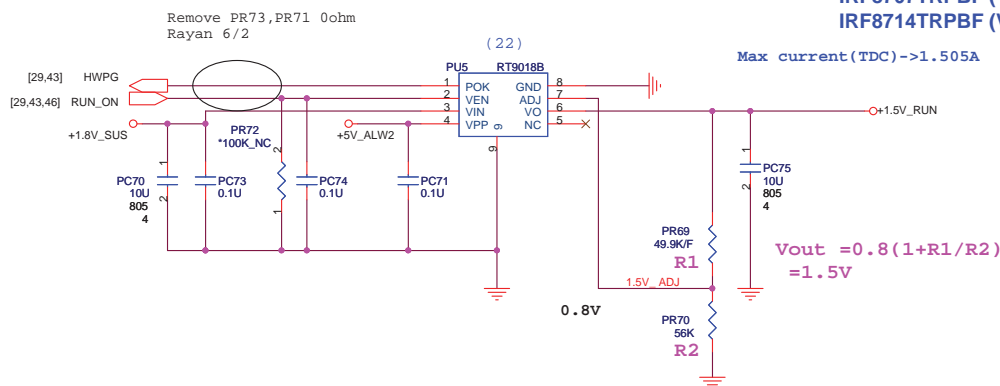
Charger (MAX8731A)

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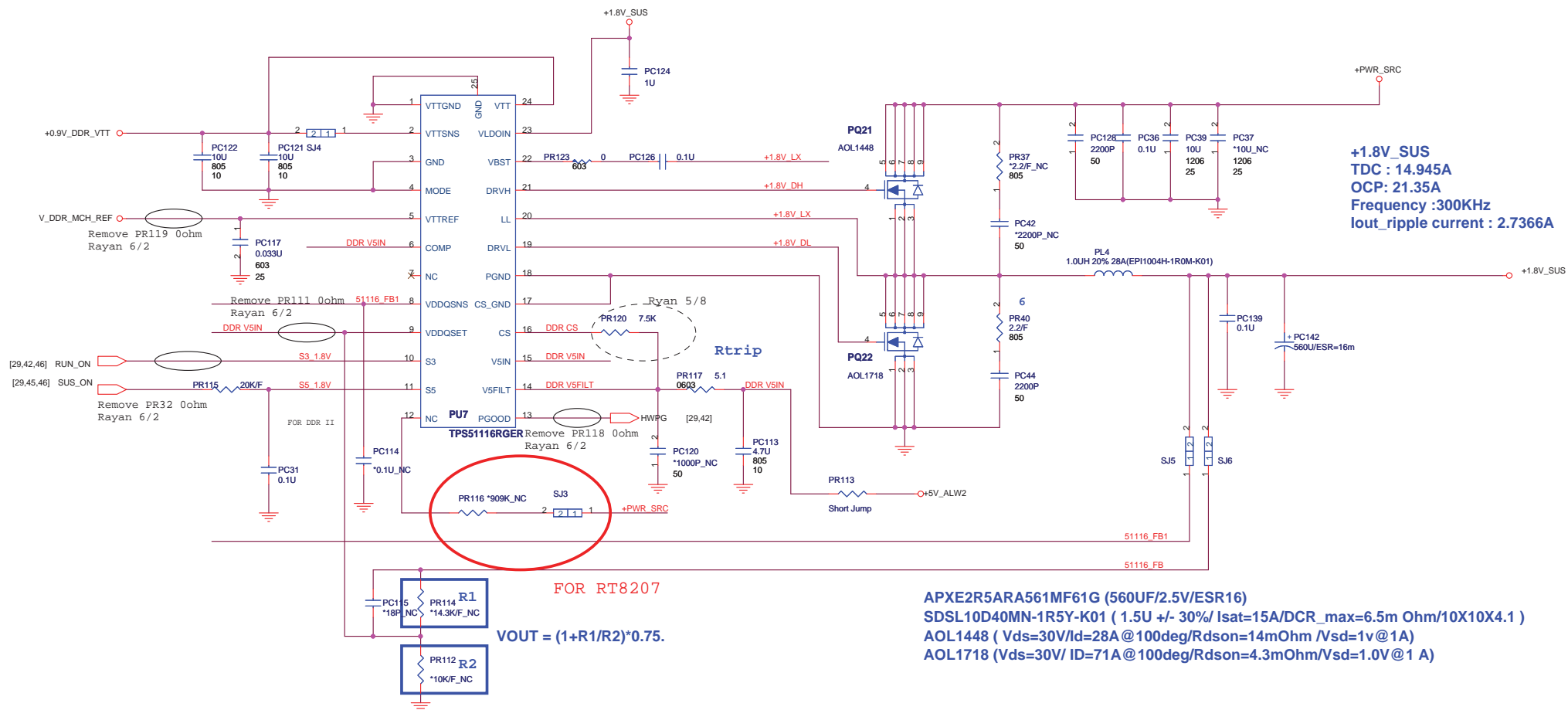
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APXE2R5ARA561MF61G (560UF/2.5V/ESR16)
 SIL104R-1R5B (1.5U +/- 30%/ Isat=10A/DCR_max=8.1m Ohm/10X10X3.8)
 IRF8707TRPBF (Vds=30V/Id=9.1A @ 75deg/Rdson=17.5mOhm)
 IRF8714TRPBF (Vds=30V/ ID=11A @ 70deg/Rdson=13mOhm/Vsd=1.0V @11A)

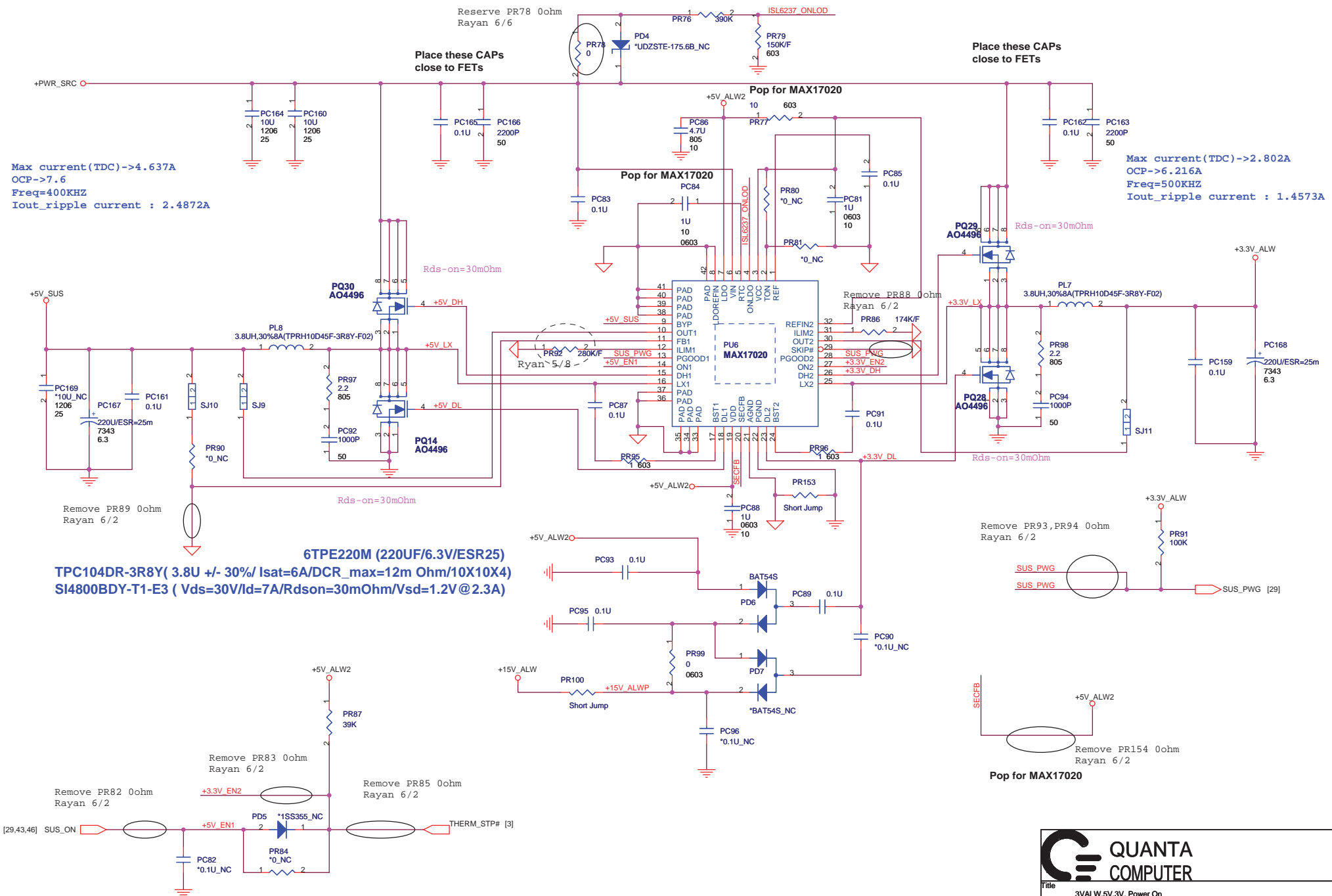



Title			1.05_VCCP & 1.5V_RUN
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DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

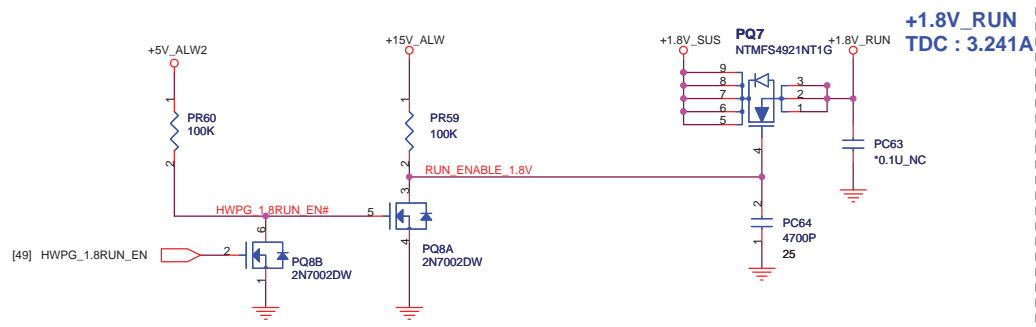
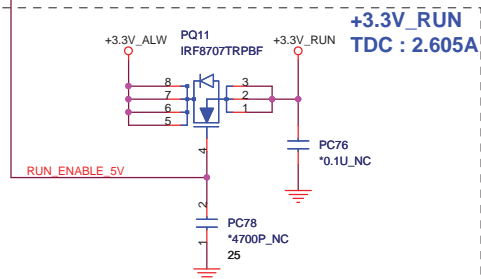
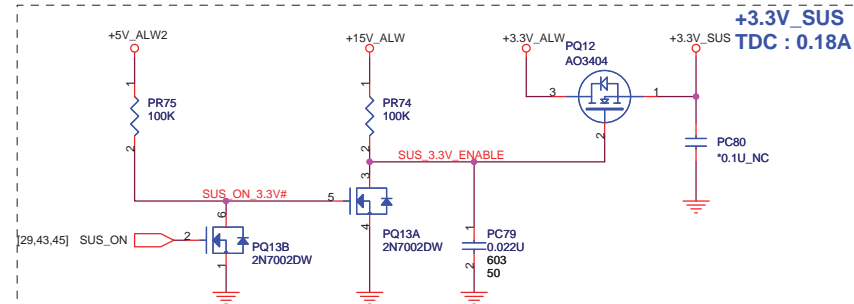
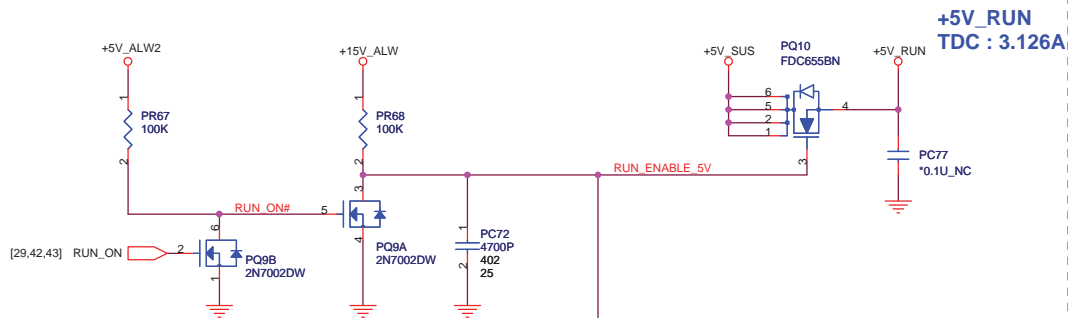




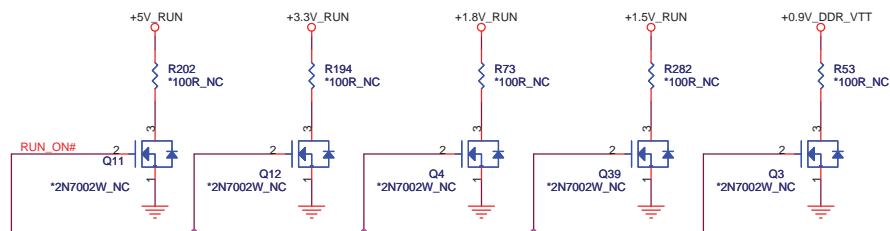
QUANTA

COMPUTER

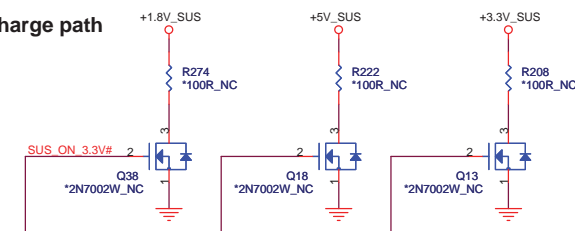
File: 3VALW.5V.3V, Power On		
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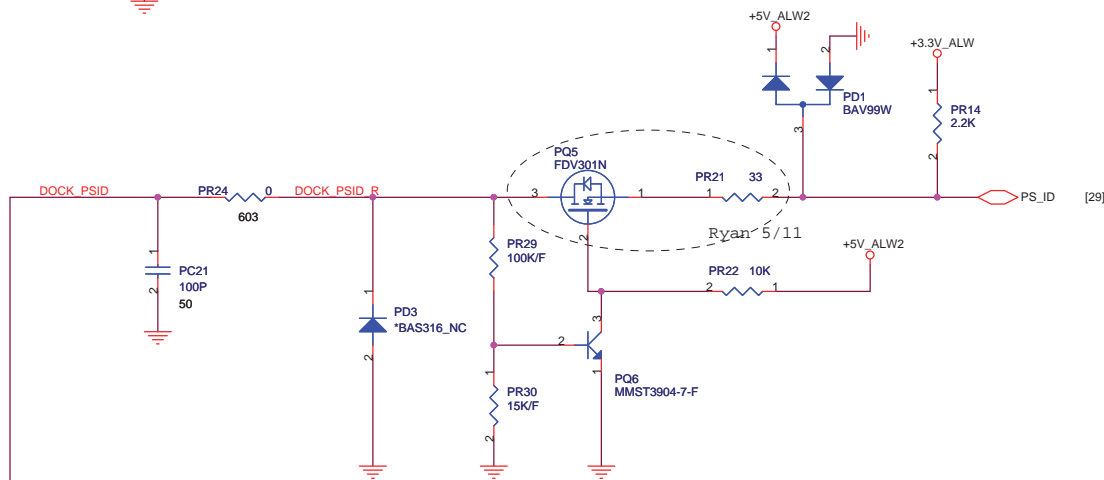
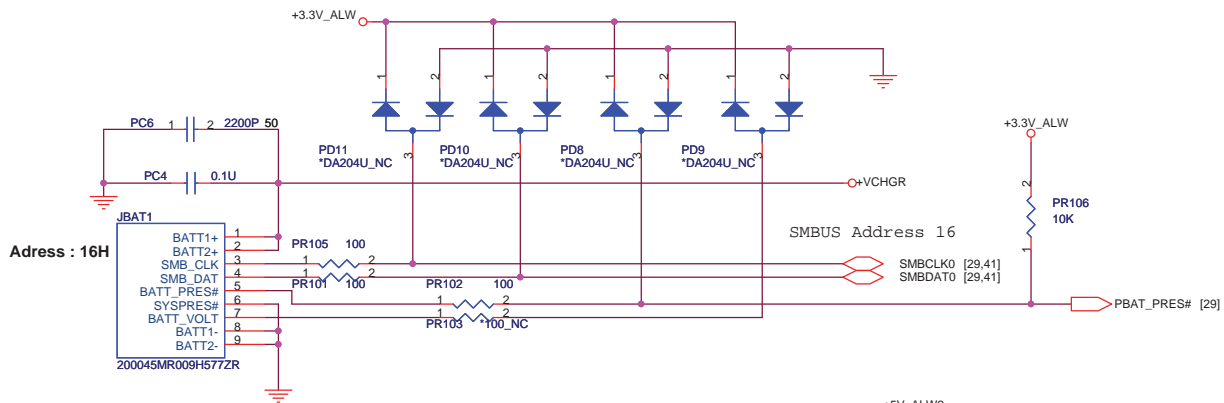
Reserve discharge path



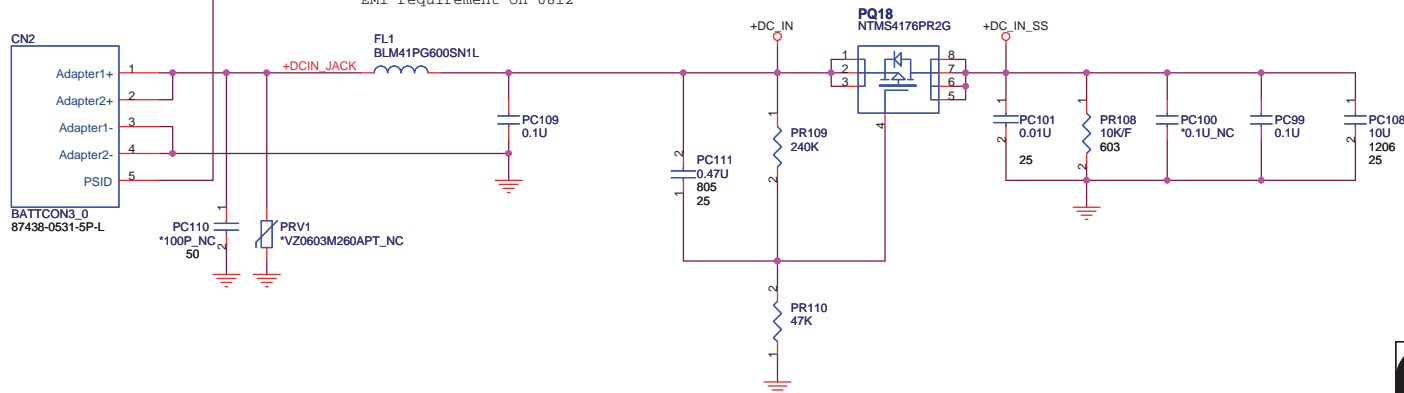
Reserve discharge path



File	RUN POWER SW		
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Change Value per GG updated
EMI requirement on 0812



Title
DCIN,BATT CONNECTOR

Size
Document Number
M8G

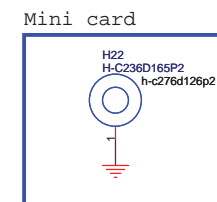
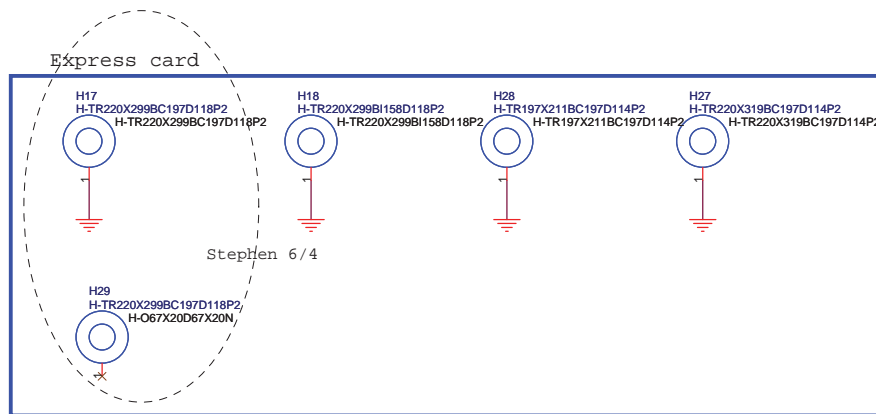
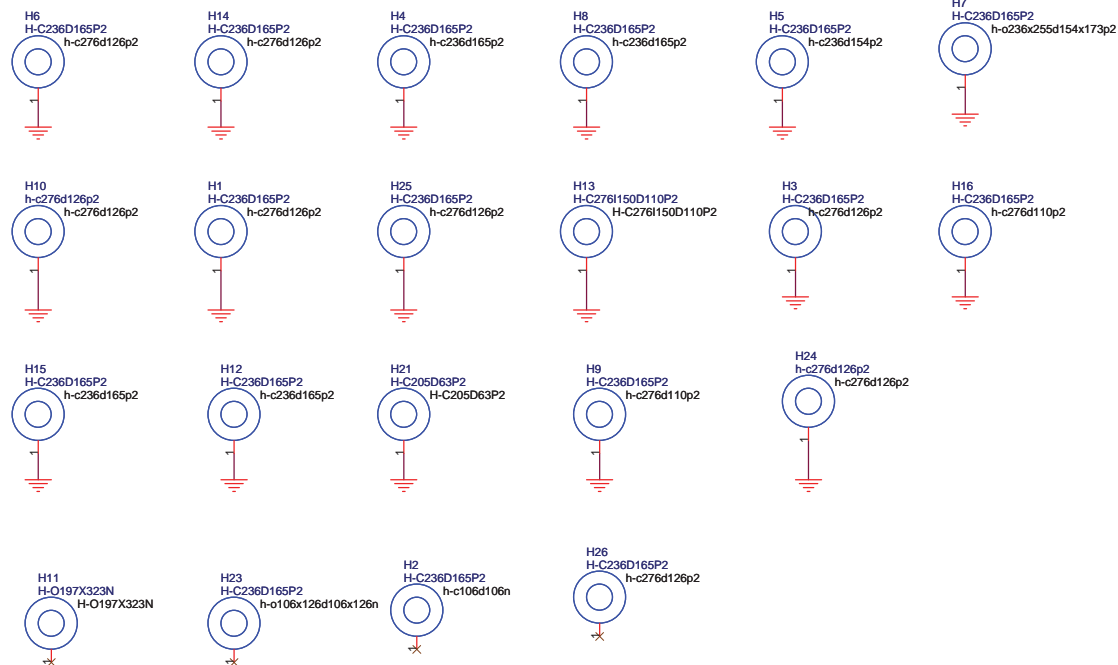
Date: Tuesday, June 02, 2009

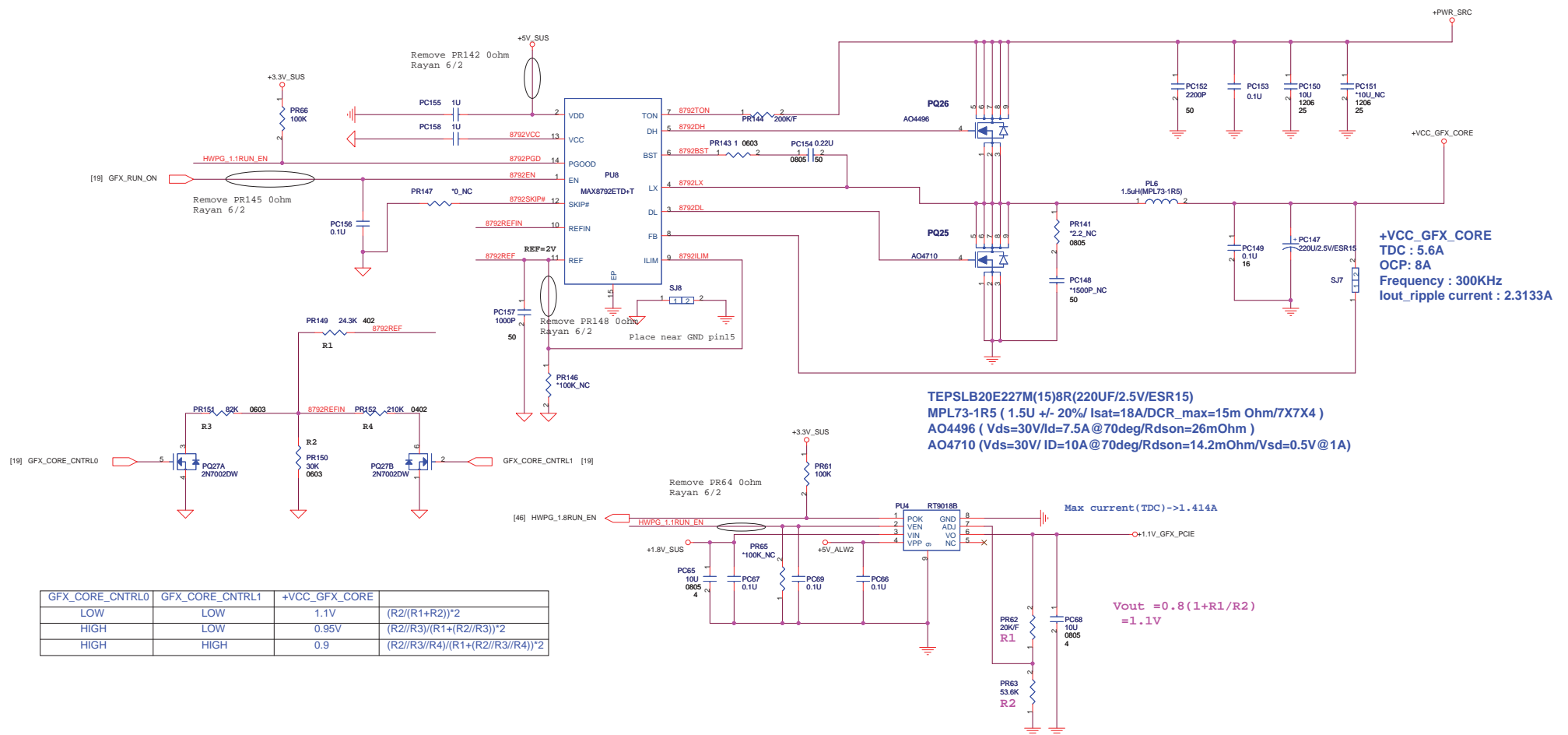
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1B


<http://laptop-motherboard-schematic.blogspot.com/>

www.vinafix.vn





Reserved for EMI.



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EMI CAP		
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